Computationally Efficient MPC with Embedded Adaptive Battery Balancing for CHB Inverters

Filippo Gemma, *Student Member, IEEE*, Giulia Tresca, *Member, IEEE*,
Jacopo Riccio, *Member, IEEE*, Behrouz Mohammadzadeh, *Student Member, IEEE*,
Andrea Volpini, *Student Member, IEEE*, Pericle Zanchetta, *Fellow, IEEE*.

***Abstract*—This paper proposes a Tree-Based Finite-Control-Set Model Predictive Control (TBFCS-MPC) strategy for a Cascaded H-Bridge (CHB) inverter, integrated with an adaptive online Look-Up Table (LUT) for real-time battery voltage balancing. The proposed TBFCS-MPC reduces computational complexity by limiting the number of evaluated voltage vectors to a maximum of 22, compared to 127 in conventional FCS-MPC approaches. This reduction enables real-time execution on embedded hardware, achieving a cost function evaluation time of only 4.2 μs, compared to 24.1 μs with state-of-the-art solutions. The LUT dynamically selects switching states based on instantaneous battery voltages, ensuring active balancing. Experimental results validate the method's fast current reference tracking, effective balancing, and significantly reduced computational burden, making it a practical solution for high-performance, battery-fed multilevel inverter applications.**

***Index Terms*—Cascaded H-Bridge, Finite-Control-Set Model-Predictive Control, Computational Burden Reduction, Li-Ion Batteries, Batteries Balancing, Tree-Based.**

I. Introduction

Among various multilevel converter architectures, the Cascaded H-Bridge (CHB) is widely used in high-voltage applications due to its modular design, scalability, and strong fault-tolerant capabilities [1], [2]. In battery-based systems-i.e. BESS applications -, the CHB plays a critical role in energy management, helping to extend battery life, improve safety, and ensure stable power distribution [3]. These advantages necessitate a combination of precise control strategies and dynamic performance to optimize efficiency, particularly under varying load conditions [4]. Additionally, ensuring proper battery voltage balancing is essential to maintain consistent performance and protect the overall battery health. This requires an advanced control approach capable of efficiently managing the nonlinearities in battery voltage behavior.

To improve system performance by reducing power losses and enhancing control flexibility, extensive research has focused on advanced control strategies, particularly Model-Predictive Control (MPC). Over the past decades, advancements in microcontrollers have significantly increased computational power, facilitating the widespread adoption of MPC [5]. Among its variations, Finite-Control-Set Model-Predictive Control (FCS-MPC) determines the optimal control action by solving a state-space-based integer quadratic optimal control problem (IQOCP) over a predefined prediction horizon [6], [7]. The control objectives are embedded in a cost function, which balances multiple, often conflicting requirements while accounting for nonlinearities introduced by power electronic switching and electrical loads.

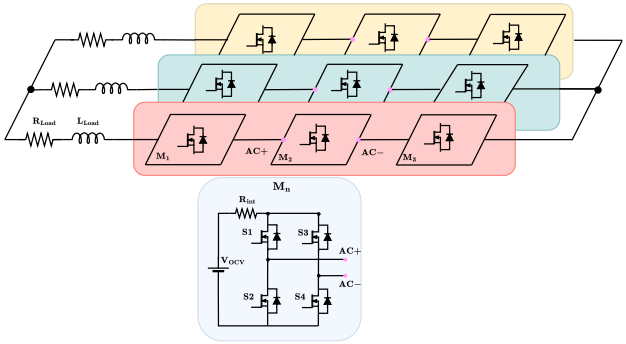


Fig. 1: Cascaded H-Bridge with Battery and Load.

Applying MPC to CHB converters introduces significant computational challenges, due to the high number of available voltage vectors (VVs) compared to conventional two-level voltage source inverters [8]. Predicting the system's future state requires a computational effort that grows with the number of feasible VVs, while redundancies in gate control signal (GCS) set further complicate control implementation. Additionally, including battery balancing into the control strategy increases the computational burden, as it introduces additional complexity in managing the nonlinearities of the battery voltage, which must be considered in real-time control decisions.

Different strategies have been suggested to reduce the computational burden. A cell-by-cell-based (CBCB) FCS-MPC approach, introduced in [9] for CHB rectifiers, independently formulates and solves the IQOCP for each H-Bridge (HB) phase module, thereby reducing the problem's complexity. Similarly, a hierarchical FCS-MPC strategy for grid-connected CHBs, proposed in [10], utilizes a $2D$ control plane to preselect candidate GCSs, effectively limiting computational requirements. Other techniques include adaptive VV set selec-

Filippo Gemma, Giulia Tresca, Behrouz Mohammadzadeh, Andrea Volpini and Pericle Zanchetta are with Electrical, Computer and Biomedical Engineering Dept., Pavia, Italy; e-mail: filippo.gemma01@universitadipavia.it, giulia.tresca@unipv.it, behrouz.mohammadzadeh01@universitadipavia.it, andrea.volpini01@universitadipavia.it, pericle.zanchetta@unipv.it

Jacopo Riccio is with the Department of Electrical and Electronic Engineering, University of Nottingham, Nottingham, UK; e-mail:Jacopo.Riccio2@nottingham.ac.uk

tion [11] and IQOCP decomposition into sub-problems [12] to prevent exponential growth in computational demands. A further optimization method in [13] leverages a branch-and-bound (BnB) algorithm to systematically reduce the computational load. More recently, [14] introduced a reduced VV candidate selection strategy, where only adjacent VVs to the previously optimal VV are considered at each control step. Additionally, an offline optimization method proposed in [15] further mitigates computational costs but lacks real-time adaptability. However, none of these methods address the issue of battery voltage balancing.

Alternatively, several studies have focused exclusively on active battery balancing [16], [17]. Traditional balancing techniques, such as PI control and sorting-based algorithms, suffer from limited accuracy and safety concerns due to indirect control and estimation errors [18], [19]. To overcome these limitations, model-based and predictive strategies have been proposed. In particular, rule-based and fault-tolerant approaches [20]–[22] have improved balancing performance at the cell and submodule levels while respecting operational constraints. Further advancements include the variable duty-cycle-based predictive control strategy presented in [23], which dynamically adjusts the duty cycle using real-time DC-link voltage feedback to ensure uniform DC source utilization. Additionally, [24] introduced a nearest-level control method to enhance voltage balancing, while [25] proposed a hierarchical distributed control architecture for CHB converters, integrating primary and secondary control layers with balancing mechanisms.

To address the dual challenge of balancing effectiveness and the nonlinear nature of battery behavior in CHB systems, more recent works have incorporated balancing-based MPC strategies. A dual-stage MPC approach has been proposed for CHB systems [26], enabling coordinated inter-arm and intra-arm balancing under operating constraints. In parallel, a single-stage MPC formulation has been developed for generic CHB systems [27], which directly optimizes the active power references of each submodule.

While these advanced MPC techniques significantly improve steady-state balancing performance, they also introduce notable computational demands. In particular, their integration with FCS-MPC can lead to high complexity [25], posing challenges for real-time implementation. Therefore, reducing the computational burden is crucial to ensure robust energy balancing under nonlinear and constrained operating conditions.

Consequently, this study introduces an enhanced Tree-Based Finite-Control-Set Model-Predictive Control (TBFCS-MPC) approach for Cascaded H-Bridge (CHB) converters used in battery-based systems. The proposed cost function is specifically designed to minimize steady-state errors while reducing computational overhead. To achieve this, an online time-varying Look-Up Table (LUT) calculation method is introduced, ensuring battery balancing and improving computational efficiency by strategically limiting switching combinations.

TABLE I: Voltage Level and Switching State of an H-Bridge

Switching State				**Output Voltage**
S_1	S_2	S_3	S_4	
1	0	0	1	$+V_{bat}$
1	0	1	0	0
0	1	0	1	0
0	1	1	0	$-V_{bat}$

This work builds upon [8] and introduces the following contributions compared to existing strategies:

- Reduction of Computational Cost. The proposed method reduces operations per control cycle by efficiently selecting feasible voltage vectors, avoiding the exponential complexity of methods like BnB [13] and reduced VV selection [14]. A hierarchical decomposition separates current control from gate signal selection, improving scalability and enabling real-time execution on low-power hardware.
- Tree-Based Search for Cost Function Optimization. The proposed method introduces a tree-based search strategy that analyzes cost function variations to dynamically narrow the solution space and reduce voltage vector evaluations. Compared to the 2D control plane approach in [10], this significantly improves decision speed and computational efficiency.
- Time-Varying Look-Up Tables for Active Balancing. The proposed method employs dynamic LUTs that update in real time based on system states, enabling effective compensation for voltage imbalances.

The paper is structured as follows: Section II introduces the system model. Section III discusses the applied control strategy. Experimental results are presented in Section IV. Finally, Section V concludes the paper, summarizing key findings and outlining future research directions.

II. Cascaded H-Bridge

The Cascaded H-Bridge multilevel converter, depicted in Fig. 1, consists of multiple H-bridge power modules connected in series on the AC side. The total number of switching state combinations for a three-phase CHB inverter with N_{mod} Half-Bridge cells can be computed as:

$$N_{swc} = 2^{N_{mod}} \tag{1}$$

The H-Bridge output voltage as function of its switching states can be written as shown in Table I. S_1, S_2, S_3, and S_4 are the switching states, which can be either 1 or 0, depending on whether the device is on or off, respectively. The output voltage can be expressed as [28]:

$$V_{out} = V_{bat}\left(\frac{1}{2}(S_1 + S_4) - \frac{1}{2}(S_2 + S_3)\right) \tag{2}$$

where V_{out} and V_{bat} represent the output voltage of the H-bridge and the battery pack voltage, respectively.

In battery-based systems, each H-bridge module is typically powered by an individual battery pack serving as its DC

TABLE II: Battery and Load values.

Variable	Symbol	Value	Unit
Bat. Nom. Volt.	V_{bat}	4.2	V
Bat. Capacity	C_{bat}	2	Ah
Bat. Int. Res.	R_{int}	18	$m\Omega$
Bat. in parallel	#	2	#
Bat. in series	#	11	#
Bat. Pack Volt.	$V_{batPack}$	46.2	V
Bat. Pack Capacity	$C_{batPack}$	4	Ah
Bat. Pack Res.	$R_{intPack}$	9	$m\Omega$
Load Res.	R_{Load}	10	Ω
Load Ind.	L_{Load}	5	mH

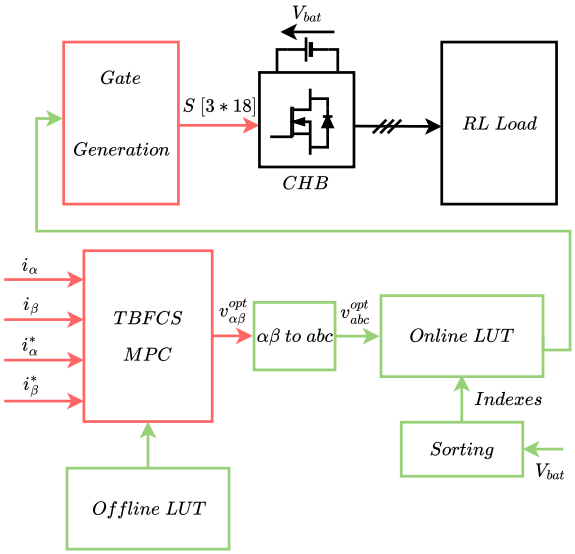


Fig. 2: Schematic of the proposed control: (red) TBFCS-MPC and Gate Generation selection; (green) offline and online LUT generation; (black) power system composed of Li-Ion Batteries, CHB and RL load.

source. The number of voltage levels (m) in a CHB inverter can be calculated as:

$$m = 2H + 1 \tag{3}$$

where H is the number of H-bridge cells per phase leg. The total number of active switches (N_{sw}) can be determined as:

$$N_{sw} = 6(m - 1) \tag{4}$$

The system analyzed in this work consists of a CHB converter with three submodules (SMs) per phase, each powered by a Li-Ion battery pack. The converter supplies a resistive-inductive (RL) load, as shown in Fig. 1. The system parameters are provided in Table II. The number of possible switching combinations reaches $2^{18} = 262144$ for three H-bridges per phase ($N_{mod} = 18$). This exponential growth poses a significant computational challenge for real-time control and optimization algorithms, making efficient control strategies such as predictive control with LUTs essential for practical implementations.

III. Control Strategy

The defining equations of the system in the $\alpha\beta$ frame are given by:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = R_{Load} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + L_{Load} \frac{d}{dt} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5}$$

where L_{Load} and R_{Load} are the load inductance and resistance, respectively. i_α and i_β are the α- and β-axis currents, while v_α and v_β are the $\alpha\beta$ components of the CHB output voltage.

The Tree-Based Finite-Control-Set Model-Predictive Control algorithm selects the optimal voltage vector $v^{opt}_{\alpha\beta}$ to be applied to the system. This approach allows the controller to quickly narrow down the best control action without exhaustively testing all possibilities, significantly reducing computation time. The optimal voltage vector $v^{\text{opt}}_{\alpha\beta}$ is determined through a directional search performed in the first stage of the control algorithm. This stage identifies the voltage vector (VV) that minimizes the cost function and aligns the system response with the reference trajectory. This direction corresponds to the one in which the cost function associated with the prediction reaches its minimum.

Simultaneously, the TBFCS-MPC integrates a dual-layer Look-Up Table (LUT) architecture that supports both voltage vector selection and battery balancing. The first layer consists of an offline-generated look-up table (LUT) that stores all admissible voltage vectors, filtered to exclude redundancies, and mapped in the $\alpha\beta$ reference frame. The second layer is an online LUT used in real time to determine the gate signals and manage battery balancing actions, based on the current system state and selected switching pattern. The interaction between the two layers enables efficient control decisions while maintaining active balancing functionality. The overall control strategy is illustrated in Fig. 2.

A. *Offline LUT*

An initial Look-Up Table (LUT) is generated offline to include all admissible and non-redundant voltage vectors in the $\alpha\beta$ plane. This LUT is built by evaluating every possible switching combination of the multilevel converter's submodules. For each combination, the output voltage is calculated and then mapped to the $\alpha\beta$ reference frame using the Clarke transformation. To eliminate redundancy, only voltage vectors corresponding to unique positions in the $\alpha\beta$ plane are retained. Switching combinations that produce identical vectors, despite differing states, are discarded. The resulting LUT forms a compact and optimized dataset that supports faster online control decisions, while ensuring that only physically valid and non-redundant vectors are considered during real-time optimization.

The LUT is organized as a 127×2 matrix, with each row representing the α and β components of a unique voltage vector. These vectors are chosen not only to eliminate redundancy but also to enhance robustness in the presence of modeling uncertainties. Specifically, the selected vectors

span the converter's expected operating range, accounting for variations such as battery voltage fluctuations. This selection strategy ensures adequate resolution across the $\alpha\beta$ plane, preserving control accuracy while significantly reducing the number of combinations evaluated during online operation.

This offline LUT defines the search space for the Tree-Based FCS-MPC, enabling efficient identification of the optimal voltage vector at each control cycle. As a result, the search remains computationally efficient and confined to physically meaningful regions.

B. Tree-Based FCS-MPC

A Tree-Based Finite-Control-Set Model-Predictive Control, depicted in Fig. 3, is applied to determine the optimal voltage vector $v_{\alpha\beta}^{opt}$ to apply to the system. The cost function used in the TBFCS-MPC algorithm is defined as:

$$g\left(n\right) = \left|\left|{\mathbf{i}_{\alpha,\beta}}^{*} - {\mathbf{i}_{\alpha,\beta}}^{k+1}(n)\right|\right|_{2}^{2} \tag{6}$$

where $g(n)$ represents the squared two-norm of the error between the reference current vector ${\mathbf{i}_{\alpha,\beta}}^{*}$ and the predicted current vector ${\mathbf{i}_{\alpha,\beta}}^{k+1}(n)$ at the next sampling instant $k+1$. The goal of the controller is to minimize the cost function (6) to achieve accurate current tracking.

The index n represents the combination, where each combination corresponds to a specific pair of $\alpha\beta$ voltages $v_\alpha(n)$ and $v_\beta(n)$ generated by the CHB inverter. Combinations are considered only if they are explicitly tested during the search process.

The predicted current values ${\mathbf{i}_{\alpha,\beta}}^{k+1}(n)$ are computed based on the RL load model, discretized using the forward Euler approximation [29]. The prediction equations in the $\alpha\beta$ reference frame are:

$$\begin{bmatrix} i_\alpha^{k+1} \\ i_\beta^{k+1} \end{bmatrix} = (1 - \frac{T_s R_{Load}}{L_{Load}}) \begin{bmatrix} i_\alpha^{k} \\ i_\beta^{k} \end{bmatrix} + \frac{T_s}{L_{Load}} \begin{bmatrix} v_\alpha(n) \\ v_\beta(n) \end{bmatrix} \tag{7}$$

where i_α^k and i_β^k are the α- and β-axis currents at the k-instant sampling step, while $v_\alpha(n)$ and $v_\beta(n)$ are the $\alpha\beta$ voltage components generated by the CHB for the n-th switching combination.

Fig. 3 shows the search process for the optimal voltage vector, which is based on a hierarchical, layer-wise strategy. Each layer corresponds to a subset of voltage vectors that the CHB can produce. Given the 7-level structure of the CHB, the search spans up to 6 layers, as the seventh level represents the zero vector. By organizing the search in layers, the control algorithm systematically narrows down the number of evaluated voltage vectors combinations. In higher-level CHB configurations, this tree-based organization ensures that the number of tested vectors does not grow exponentially but remains predictably bounded. This property makes the approach scalable and keeps execution times feasible even when additional submodules per phase are included. This layered approach enables a significant reduction in computational effort while maintaining accurate reference tracking and effective control performance.

As shown in Fig. 3, the search process starts with an evaluation of the possible solutions on the first layer. The optimal search direction is determined by the voltage vector that minimizes the cost function defined in (6).

Once the optimal direction is established, the search proceeds to the next layer, where only the adjacent vectors closest to the previously selected vector are tested. The path is shown in Fig. 3. The search process continues iteratively through the subsequent layers until the closest feasible voltage vector to the reference is identified. When the optimal search process is completed, the voltage vector $v_{\alpha\beta}^{opt}$ that corresponds to the minimum value of the cost function in (6) is the value applied to the system at the next control step $k+1$.

This layered search strategy reduces the total number of switching combinations that needs to be evaluated. In a conventional finite control set MPC, the total number of possible switching combinations for a 7-level CHB would be 127 [8].

However, the proposed method reduces this to a maximum of 22 combinations, as illustrated in Fig. 4(b), by applying an enhanced layered search strategy. This substantial reduction in the search space significantly lowers the computational burden, enabling faster and more efficient real-time current control. Under light-load conditions, even fewer voltage vectors (VVs) are evaluated, as shown in Fig. 4(a). In this scenario, the search terminates after 14 iterations because the cost function values in the subsequent layer (the fourth) exceed the minimum value already identified in the previous layer. As a result, the optimal solution is selected from the third layer, as it offers the closest match to the reference.

C. Online LUT

After the TBFCS-MPC identifies the optimal voltage vector, the controller must determine the corresponding 1×18 gate signal configuration (i.e., ON/OFF states for each half-bridge) that generates the vector while supporting battery voltage balancing. This task is managed by an adaptive online LUT, which dynamically identifies the most suitable switching pattern based on real-time battery voltage measurements. The selection process is illustrated in Fig. 5.

While the offline LUT exhaustively stores all possible voltage vector combinations, the online LUT is introduced to reduce the computational burden in real time. Instead of repeatedly solving the optimization for scenarios that share similar operating conditions, these cases are precomputed and stored in the online LUT. In this way, the controller can directly retrieve the corresponding switching pattern without rerunning the optimization, ensuring both speed and consistency. The real-time task of the controller is then limited to selecting which battery module should supply the voltage, based on a ranking derived from ADC measurements—i.e., choosing the module with the highest voltage in the discharge phase. This same principle applies to negative voltages and bypass states across all phases.

First, the battery voltages are measured and stored as a vector:

$$\mathbf{v_{bat}} = \begin{bmatrix} v_{bat,1} & v_{bat,2} & \cdots & v_{bat,N} \end{bmatrix}^T \tag{8}$$

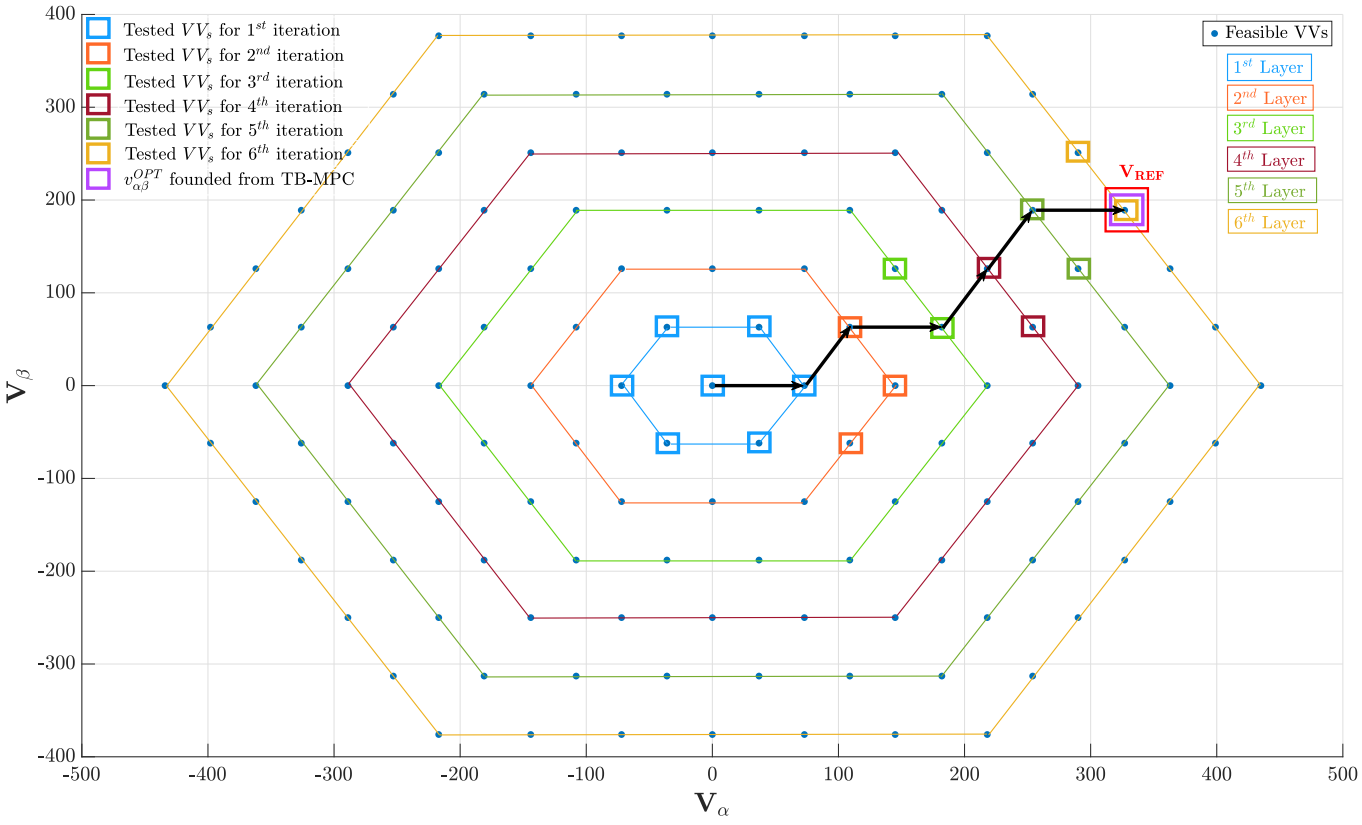


Fig. 3: Tree-Based FCS-MPC searching process.

where N is the number of battery modules.

The ranking operation is then performed by sorting the battery voltages in descending order ($\mathbf{v_{bat}}^{sorted}$). Each phase output requirement is mapped to a predefined switching template $\mathbf{G}_{template}$, and the selected battery module index is assigned according to the sorted list:

$$\mathbf{G}_{phase} = \mathbf{G}_{template}(\mathbf{v_{bat}}^{sorted}) \tag{9}$$

Thus, the final gate signal vector $\mathbf{G}$ is composed by concatenating the gate signals for the three phases:

$$\mathbf{G} = [\mathbf{G}_A \parallel \mathbf{G}_B \parallel \mathbf{G}_C] \tag{10}$$

where $\parallel$ denotes the concatenation operator. This process ensures that the final gate pattern both realizes the required output voltage and simultaneously promotes balancing among the battery modules.

The online LUT performs the following tasks in real time:

1) Descending sorting the battery voltages.
2) Assigns the highest-voltage modules to active paths based on the optimal voltage vector.
3) Retrieves the precomputed switching pattern corresponding to the required phase output.

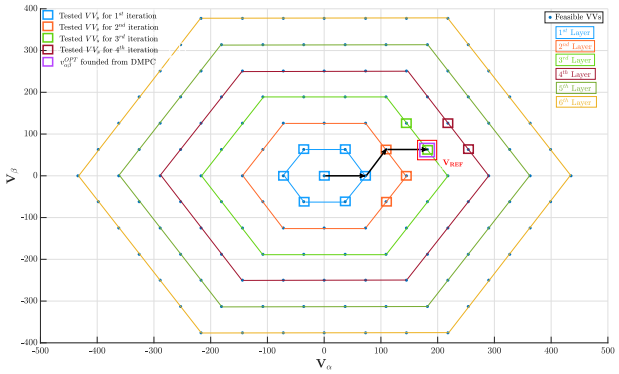
Overall, the combination of the offline LUT and the online LUT ensures that both prediction and actuation are optimized separately, preserving computational efficiency while maintaining precise control and balancing performance. The control scheme, including the two LUT layers and their interaction, is shown in Fig. 2.

IV. Experimental Results

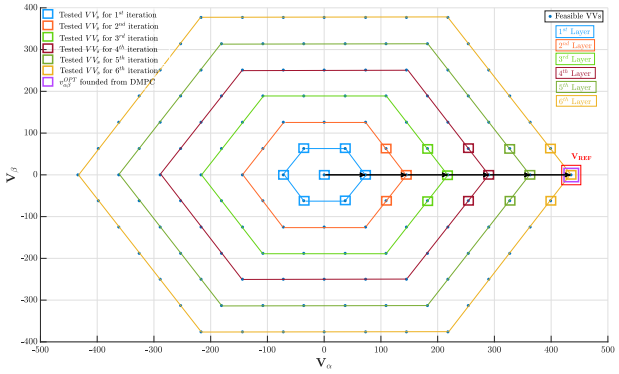
The experimental setup is shown in Fig. 6. The test bench consists of a CHB feeding an RL load and measuring instruments. The CHB is composed of three H-Bridge modules per phase, enabling the generation of seven output voltage levels. Each H-Bridge is built using MOSFET power modules (IPP320N20N3G). The commutation dead-time is set to 1.5 μs. Nine battery packs, each configured as 11s2p with Li-Ion cells (INR18650-20R), provide the DC-link voltage. The control sample time T_s is set to 5×10^{-5} s (i.e. 20 kHz). The control platform is the uCube [30]. The system parameters are summarized in Table II. The battery voltages are acquired, transferred to a PC via the UART communication protocol, and plotted on MATLAB, while the current and phase voltages are measured using an oscilloscope.

A. Computational Time Comparison

The evaluation time of the cost function— the most computationally demanding task in model predictive control—



(a)



(b)

Fig. 4: Tree-Based searching process examples: (a) 14 iterations; (b) 22 iterations.

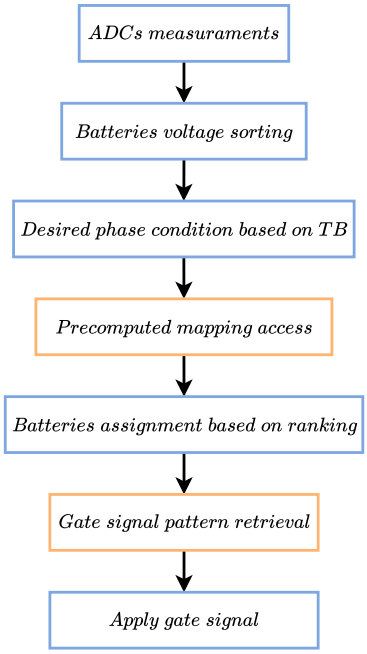


Fig. 5: Schematic of the online LUT gate signal generation: (blue) online decisions and computations; (yellow) offline decisions and computations.

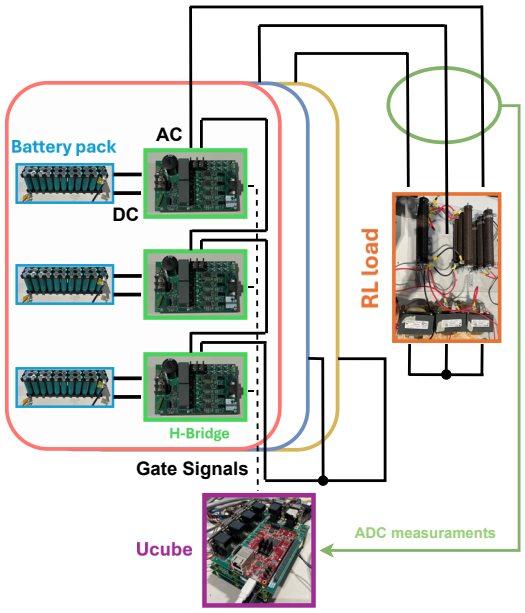


Fig. 6: Test rig.

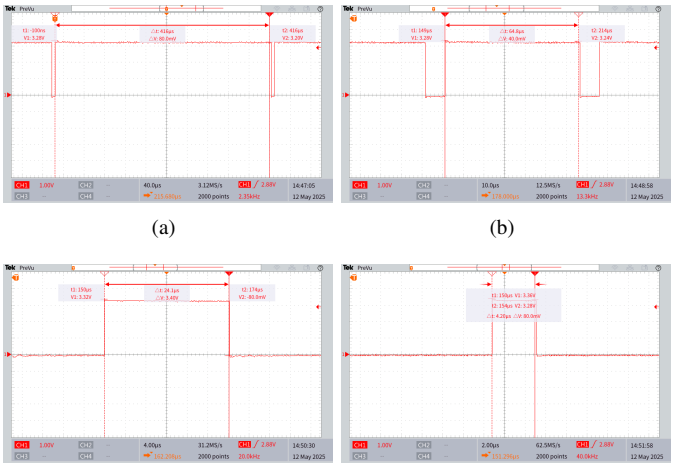
was carefully measured and experimentally verified using an oscilloscope. All experimental validations were carried out on the uCube control platform [30]. The time comparison results are presented in Table III.

Specifically, when evaluating all possible switching combinations in the control algorithm, a total of 2197 configurations are tested in each control cycle. This number comes from considering all VV combinations, removing only the redundancies related to battery bypass switching gate states. This case is used as a baseline to evaluate the computational cost of the cost function alone, helping to show how demanding a full search can be for the microcontroller. The measured computation time is 416 μs, as shown in Fig. 7(a).

To reduce the computation time, a first simplification is applied by limiting the number of allowed switching combinations. In this case, only 343 combinations are considered, corresponding to 7^3 configurations with a reduced set of voltage vectors for each phase. The corresponding computation time drops to 64.8 μs, as shown in Fig. 7(b). This result is consistent with previous findings in [15], confirming the validity of this optimization method.

A further reduction is achieved by applying stricter selection rules, resulting in a set of only 127 voltage vectors. In this case, redundancies in generating the same voltage vector are removed; each vector in the $\alpha\beta$ plane corresponds to a unique switching combination. As shown in Fig. 7(c), this approach lowers the computation time to 24.1 μs, consistent with the results reported in [8].

Finally, the proposed Tree-Based selection strategy is used to further reduce the search effort. This method evaluates a



(a) (b) (c) (d)

Fig. 7: Controller computational time for the MPC at 20 kHz: (a) time with 2197 iterations; (b) time with 343 iterations [15]; (c) time with 127 iterations [8]; (d) time with the proposed technique.

TABLE III: Controller computational time for the MPC at 20 kHz.

Number of Iterations	Time [μs]
2197	416
343 [15]	64.8
127 [8]	24.1
22	4.2

maximum of 22 candidate vectors. As a result, the computation time is reduced to just 4.2 μs, as illustrated in Fig. 7(d). Despite the smaller search space, the controller still selects the correct switching states, ensuring good performance.

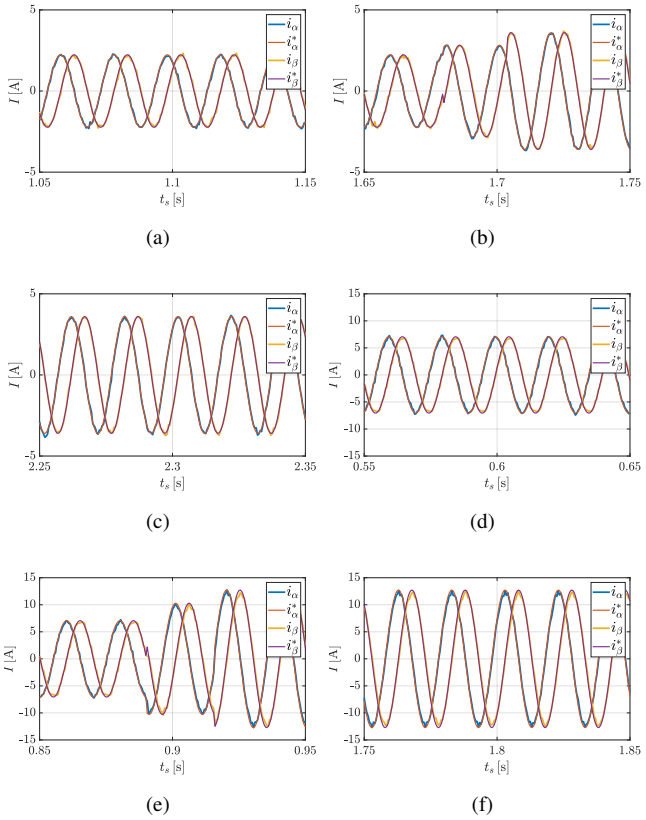
It should be noted that the reported computational times were measured during the actual run state of the microcontroller and not in idle conditions. The evaluation was carried out under steady-state operation, which represents the worst-case scenario in terms of computational demand. In this configuration, the number of tested vectors consistently reached the maximum value of 22, as also confirmed in Fig. 4(b), thereby validating the deterministic and predictable execution time of the proposed method.

The reduction in computation time is directly linked to the lower number of VVs analyzed in each cycle. This is especially important for applications that require fast control loops and high dynamic performance, such as power converters. The proposed method allows for fast execution with limited hardware resources, making it suitable for real-time embedded control.

B. Hardware Results

The experimental tests are designed to evaluate both the dynamic response of the proposed control strategy to step changes in the reference and the long-term performance of the online look-up table-based balancing algorithm.

Fig. 8, 9, 10, and 11 present a comprehensive set of experimental results obtained using the developed control

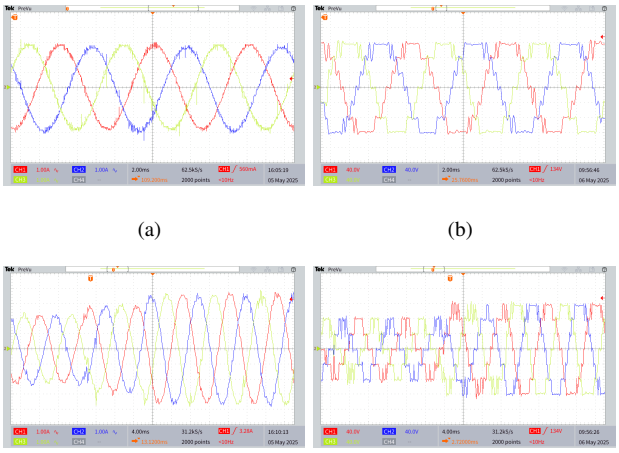


(a) (b) (c) (d) (e) (f)

Fig. 8: $i_{\alpha,\beta}$ current reference tracking: (a) Steady state; (b) Step; (c) Steady state; (d) Steady state; (d) Step; (d) Steady state.

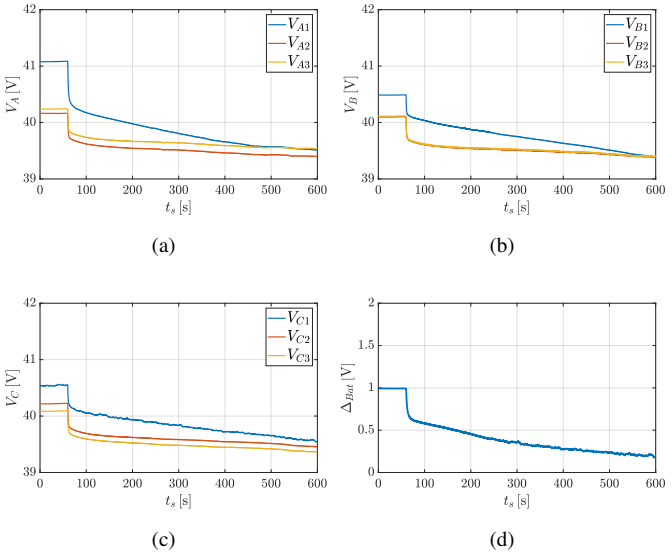
architecture. These results provide a thorough assessment of the behavior of the phase currents, output voltages, and battery module voltages during converter operation. It is observed that the phase currents accurately track their reference trajectories in all test scenarios, while the battery voltages are dynamically equalized in real time. The active balancing improves system reliability, ensures optimal energy distribution among battery packs, and contributes to an overall enhancement of performance.

Fig. 8 illustrates the tracking behavior of the α-β current components (i_α, i_β) under both low and nominal current conditions. In the first scenario, corresponding to low current operation, a step in the reference is applied at approximately $t = 1.7$ s. Fig. 8(a) and 8(c) show the steady-state current response before and after the step, respectively. Fig. 8(b) depicts the dynamic response to the step. The controller successfully tracks the reference with fast and accurate dynamics. In the second scenario, at nominal current levels, the steady-state behavior is illustrated in Fig. 8(d) and 8(f), while the dynamic response to a reference step applied at around $t = 0.9$ s is shown in Fig. 8(e). Overall, the controller demonstrates excellent tracking performance and dynamic behavior. The results confirm the high fidelity of the output currents, with very low total harmonic distortion (THD) across all phases. Specifically, the measured THD values are 1.1003% for i_a,



(a) (b) (c) (d)

Fig. 9: Oscilloscope results: (a) Phase currents i_A, i_B, and i_C at steady state; (b) CHB phase output voltages at steady state; (c) Phase currents i_A, i_B, and i_C during reference steps; (d) CHB phase output voltages during reference steps.



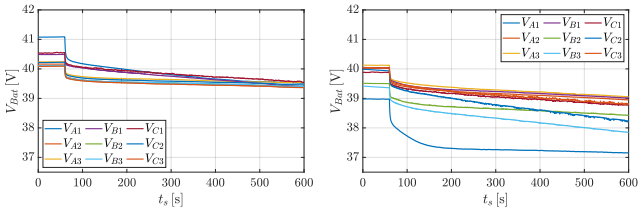
(a) (b) (c) (d)

Fig. 10: Long test experimental results: (a) Phase A battery voltages; (b) Phase B battery voltages; (c) Phase C battery voltages; (d) ΔV battery pack.

1.0168% for i_b, and 0.9979% for i_c. These values indicate that the proposed control method maintains a high-quality sinusoidal waveform with minimal harmonic distortions.

Fig. 9 shows both steady-state and transient waveforms of the three-phase output currents (i_A, i_B, and i_C), at 50 Hz, and the corresponding CHB phase voltages. Specifically, Fig. 9(a) confirms the expected sinusoidal steady-state behavior of the output currents, validating the effectiveness of the control scheme under nominal conditions. The response to a step change in the current reference is shown in Fig. 9(c), where the transient is well managed without overshoot.

In parallel, Fig. 9(b) and 9(d) show the phase voltages at the



(a) (b)

Fig. 11: Long test experimental results: Online LUT control (a) activated and (b) not activated.

CHB output. The staircase waveform typical of multilevel converters is visible. In particular, Fig. 9(b) displays the steady-state voltage waveform, while Fig. 9(d) captures the dynamic response of the output voltage during a load transition. It is noteworthy that during the step, the number of series-connected modules increases from two to three, indicating that the controller appropriately modifies the switching states to satisfy the new current demand.

The battery voltage behavior during operation is presented in Fig. 10(a) for Phase A. The voltages exhibit a smooth and gradual decrease associated with battery discharge under load conditions, indicating the successful management of energy balancing. Consistent behaviors are observed for Phases B and C in Fig. 10(b) and 10(c), respectively, confirming that the balancing strategy achieves uniform operation across all three phases.

Fig. 11 demonstrates the effectiveness of the online LUT-based balancing implementation. When the LUT-based strategy is active, as shown in Fig. 11(a), an initially unbalanced battery condition is gradually corrected. In contrast, when the LUT balancing is disabled (Fig. 11(b)), the imbalance remains unchanged over time, underscoring the necessity and impact of the proposed balancing method.

Overall, the experimental results validate the cability of the proposed control strategy to regulate both currents and battery voltages effectively. The accurate current reference tracking, the uniform and symmetric steady-state operation, and the active voltage balancing across all phases collectively demonstrate the robustness and reliability of the control system. Furthermore, the reduction in the number of switching combinations directly contributes to a significant improvement in computational efficiency, leading to faster real-time control execution and better scalability for applications requiring high dynamic performance.

V. Conclusion

This paper presented a Tree-Based Finite-Control-Set Model-Predictive Control strategy for a Cascaded H-Bridge inverter, combined with an online Look-Up Table approach for battery balancing. The proposed TBFCS-MPC algorithm significantly reduces the computational complexity by adopting a layered search strategy, which limits the number of evaluated voltage vectors to a maximum of 22. This reduction leads to

a remarkable decrease in computational time, improving the real-time feasibility of the control strategy.

The adaptive LUT approach ensures active battery balancing during operation by dynamically selecting the optimal switching state based on real-time battery voltage measurements. This guarantees balanced battery utilization while maintaining optimal performance of the inverter.

Experimental results validated the effectiveness of the proposed control strategy. The measured computational time of $4.2\ \mu s$ confirms the efficiency of the algorithm, demonstrating a significant improvement over conventional approaches. It should be emphasized that the experimental validation was intentionally performed under RL load conditions to clearly demonstrate the operation of the proposed strategy. Nonetheless, the methodology is not limited to this scenario. The LUT-based balancing and tree-based search framework is inherently scalable and can be extended to grid-connected operation with voltage/frequency variations, non-linear loads, or even faulty/degraded submodules. Such scenarios represent a natural direction for future investigation.

The proposed TBFCS-MPC with online LUTs provides an effective and computationally efficient solution for CHB inverter control, ensuring fast response, high accuracy, and improved battery management.

ACKNOWLEDGMENT

This work was supported by the Marie Skłodowska-Curie Actions (MSCA) under the European Union's Horizon 2020 Research and Innovation Staff Exchange (RISE) under Grant 872001.

REFERENCES

[1] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular multilevel converters: Recent achievements and challenges," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, DOI 10.1109/OJIES.2021.3060791, pp. 224–239, 2021.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, DOI 10.1109/TIE.2010.2049719, no. 8, pp. 2553–2580, 2010.

[3] F. Gemma, G. Tresca, A. Formentini, and P. Zanchetta, "Balanced charging algorithm for chb in an ev powertrain," *Energies*, vol. 16, DOI 10.3390/en16145565, no. 14, 2023. [Online]. Available: https://www.mdpi.com/1996-1073/16/14/5565

[4] G. Tresca, A. Formentini, J. Riccio, N. Anglani, and P. Zanchetta, "A reconfigurable cascaded multilevel converter for ev powertrain," *IEEE Transactions on Industry Applications*, vol. 60, DOI 10.1109/TIA.2023.3337763, no. 2, pp. 3332–3344, 2024.

[5] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2016.2625238, no. 2, pp. 935–947, 2017.

[6] P. Karamanakos and T. Geyer, "Guidelines for the design of finite control set model predictive controllers," *IEEE Transactions on Power Electronics*, vol. 35, DOI 10.1109/TPEL.2019.2954357, no. 7, pp. 7434–7450, 2020.

[7] A. Volpini, S. R. D. Salvo, G. Tresca, R. Leuzzi, and P. Zanchetta, "A unified modulated model predictive control for a two-stage ac-dc converter interfacing a vanadium redox flow battery," *IEEE Transactions on Industry Applications*, DOI 10.1109/TIA.2025.3548583, pp. 1–11, 2025.

[8] F. Gemma, J. Riccio, G. Tresca, A. Volpini, and P. Zanchetta, "Finite-control-set model predictive control with reduced computational burden in cascaded h-bridge permanent magnet synchronous motor drives for ev applications," in *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, DOI 10.1109/ECCE55643.2024.10861662, pp. 3941–3947, 2024.

[9] C. Qi, X. Chen, P. Tu, and P. Wang, "Cell-by-cell-based finite-control-set model predictive control for a single-phase cascaded h-bridge rectifier," *IEEE Transactions on Power Electronics*, vol. 33, DOI 10.1109/TPEL.2017.2677500, no. 2, pp. 1654–1665, 2018.

[10] T. He, M. Wu, R. P. Aguilera, D. D.-C. Lu, Q. Liu, and S. Vazquez, "Low computational burden model predictive control for single-phase cascaded h-bridge converters without weighting factor," *IEEE Transactions on Industrial Electronics*, vol. 70, DOI 10.1109/TIE.2022.3167133, no. 3, pp. 2396–2406, 2023.

[11] P. Karamanakos, K. Pavlou, and S. Manias, "An enumeration-based model predictive control strategy for the cascaded h-bridge multilevel rectifier," *IEEE Transactions on Industrial Electronics*, vol. 61, DOI 10.1109/TIE.2013.2278965, no. 7, pp. 3480–3489, 2014.

[12] Y. Zhang, X. Wu, X. Yuan, Y. Wang, and P. Dai, "Fast model predictive control for multilevel cascaded h-bridge statcom with polynomial computation time," *IEEE Transactions on Industrial Electronics*, vol. 63, DOI 10.1109/TIE.2016.2572662, no. 8, pp. 5231–5243, 2016.

[13] Y. Zhang, X. Wu, and X. Yuan, "A simplified branch and bound approach for model predictive control of multilevel cascaded h-bridge statcom," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2017.2698360, no. 10, pp. 7634–7644, 2017.

[14] Q. Xiao, Y. Jin, H. Jia, Y. Mu, Y. Ji, R. Teodorescu, and F. Blaabjerg, "Modulated model predictive control for multilevel cascaded h-bridge converter-based static synchronous compensator," *IEEE Transactions on Industrial Electronics*, vol. 69, DOI 10.1109/TIE.2021.3056953, no. 2, pp. 1091–1102, 2022.

[15] G. Scaglione, C. Nevoloso, G. Schettino, A. O. D. Tommaso, and R. Miceli, "A novel multiobjective finite control set model predictive control for ipmsm drive fed by a five-level cascaded h-bridge inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, DOI 10.1109/JESTPE.2024.3362404, no. 2, pp. 1959–1973, 2024.

[16] F. Gemma, G. Tresca, S. R. Di Salvo, A. Formentini, and P. Zanchetta, "A novel charging approach to temperature and state of charge management in bev," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, DOI 10.1109/ECCE53617.2023.10362079, pp. 2706–2712, 2023.

[17] G. Tresca, A. Formentini, F. Gemma, F. Lusardi, R. Leuzzi, and P. Zanchetta, "Soc governed algorithm for an ev cascaded h-bridge connected to a dc charger," in *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, pp. 1–9, 2022.

[18] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-charge (soc)-balancing control of a battery energy storage system based on a cascade pwm converter," *IEEE Transactions on Power Electronics*, vol. 24, DOI 10.1109/TPEL.2009.2014868, no. 6, pp. 1628–1636, 2009.

[19] F. Gao, L. Zhang, Q. Zhou, M. Chen, T. Xu, and S. Hu, "State-of-charge balancing control strategy of battery energy storage system based on modular multilevel converter," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, DOI 10.1109/ECCE.2014.6953744, pp. 2567–2574, 2014.

[20] E. Chatzinikolaou and D. J. Rogers, "Cell soc balancing using a cascaded full-bridge multilevel converter in battery energy storage systems," *IEEE Transactions on Industrial Electronics*, vol. 63, DOI 10.1109/TIE.2016.2565463, no. 9, pp. 5394–5402, 2016.

[21] G. Liang, E. Rodriguez, G. G. Farivar, S. Ceballos, C. D. Townsend, N. B. Y. Gorla, and J. Pou, "A constrained intersubmodule state-of-charge balancing method for battery energy storage systems based on the cascaded h-bridge converter," *IEEE Transactions on Power Electronics*, vol. 37, DOI 10.1109/TPEL.2022.3170062, no. 10, pp. 12 669–12 678, 2022.

[22] H. Xue, J. He, Y. Ren, and P. Guo, "Seamless fault-tolerant control for cascaded h-bridge converters based battery energy storage system," *IEEE Transactions on Industrial Electronics*, vol. 70, DOI 10.1109/TIE.2022.3177789, no. 4, pp. 3803–3813, 2023.

[23] H. Yao, Y. Yan, Y. Cao, P. Song, and T. Shi, "A variable duty cycle-based predictive control for pmsm fed by cascaded h-bridge inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, DOI 10.1109/JESTPE.2022.3154045, no. 4, pp. 4195–4206, 2022.

[24] L. Mathe, P. Dan Burlacu, E. Schaltz, and R. Teodorescu, "Battery pack state of charge balancing algorithm for cascaded h-bridge multilevel converters," DOI 10.1109/EEEIC.2016.7555737, pp. 1–6, 2016.
[25] B. Xu, H. Tu, Y. Du, H. Yu, H. Liang, and S. Lukic, "A distributed control architecture for cascaded h-bridge converter with integrated battery energy storage," *IEEE Transactions on Industry Applications*, vol. 57, DOI 10.1109/TIA.2020.3039430, no. 1, pp. 845–856, 2021.
[26] P. Poblete, R. H. Cuzmar, R. P. Aguilera, J. Pereda, A. M. Alcaide, D. Lu, Y. P. Siwakoti, and G. Konstantinou, "Dual-stage mpc for soc balancing in second-life battery energy storage systems based on delta-connected cascaded h-bridge converters," *IEEE Transactions on Power Electronics*, vol. 40, DOI 10.1109/TPEL.2024.3461749, no. 1, pp. 500–515, 2025.
[27] G. Liang, E. Rodriguez, G. G. Farivar, E. Nunes, G. Konstantinou, C. D. Townsend, R. Leyva, and J. Pou, "Model predictive control for intersubmodule state-of-charge balancing in cascaded h-bridge converter-based battery energy storage systems," *IEEE Transactions on Industrial Electronics*, vol. 71, DOI 10.1109/TIE.2023.3290249, no. 6, pp. 5777–5786, 2024.
[28] B. Wu and M. Narimani, *Cascaded H-Bridge Multilevel Inverters*, pp. 119–141, 2017.
[29] J. Riccio, P. Karamanakos, S. Odhano, M. Tang, M. D. Nardo, G. Tresca, and P. Zanchetta, "Modulated model-predictive integral control applied to a synchronous reluctance motor drive," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, DOI 10.1109/JESTPE.2023.3245077, no. 3, pp. 3000–3010, 2023.
[30] A. Galassini, G. Lo Calzo, A. Formentini, C. Gerada, P. Zanchetta, and A. Costabeber, "ucube: Control platform for power electronics," DOI 10.1109/WEMDCD.2017.7947749, pp. 216–221, 2017.

Filippo Gemma (Student Member, IEEE) received the B.Sc. and M.Sc degrees in electrical engineering in 2020 and 2022, respectively, from the University of Pavia, Pavia, Italy, where he is currently working toward the Ph.D. degree in electrical engineering with the PELAB, the Power Electronics group at the University of Pavia. His research interests include multilevel and reconfigurable converters for automotive applications, and control of electric drives based on model-based and model-free predictive control.

Giulia Tresca (Member, IEEE) received her B.Sc. degree in Electrical Engineering from the University of L'Aquila, Italy, in 2015. She completed her M.Sc. and Ph.D. degrees in Electrical Engineering at the University of Pavia, Italy, in 2017 and 2023, respectively. From 2017 to 2019, she worked as a Test Engineer at Infineon in Villach, Austria. She is currently an Assistant Professor at PELAB, the Power Electronics Laboratory at the University of Pavia. Her research interests include multilevel and reconfigurable converters for automotive applications, battery management systems, and control of electrical drives.

Jacopo Riccio (Member, IEEE) received his B.Sc. and M.Sc. degrees in Mechanical Engineering from the University of Roma Tre, Rome, Italy, in 2014 and 2018, respectively. He completed his Ph.D. in Electrical Engineering at the University of Nottingham, UK, in 2023. Since 2023, Dr. Riccio has been a Research Fellow with the same group at the University of Nottingham. His research interests include the control of electric drives, particularly model-based predictive control and sensorless algorithms, as well as experimental characterization of internal permanent magnet and synchronous reluctance machines. He was honored with the best IEEE-IAS Prize Paper Award in 2024.

Behrouz Mohammadzadeh (Student Member, IEEE) received his B.Sc. in Electronic Engineering from Shomal University, Amol, Iran, in 2011, and his M.Sc. in Industrial Automation Engineering from the University of Pavia, Italy, in 2023. He is currently pursuing a Ph.D. at the University of Pavia, where his research focuses on modular converter designs, DC-DC converters, battery energy storage systems, and high-efficiency converter topologies for industrial and renewable energy applications.

Andrea Volpini (Student Member, IEEE) is a PhD Student at the University of Pavia, Pavia, Italy, where he received the B.Sc. and the M.Sc degrees in Industrial Engineering in 2019, and in Electrical Engineering in 2022, respectively. In 2022 he worked as a Research Assistant in PELAB, the Power Electronics group at the University of Pavia. His research interests include DC-DC isolated converters, wide band-gap semiconductors and model predictive control for power converters.

Pericle Zanchetta (M '00, SM '15, F '19) received his MEng degree in Electronic Engineering and his Ph.D. in Electrical Engineering from the Technical University of Bari (Italy) in 1993 and 1997 respectively. In 1998 he became Assistant Professor of Power Electronics at the same University. In 2001 he became lecturer in the PEMC research group at the University of Nottingham – UK, where he became Professor in Control and Power Electronics in 2013. From 2022 he is full professor of Power Electronics at the University of Pavia, Italy and part time professor at the University of Nottingham. He has published over 400 peer reviewed scientific papers. Professor Zanchetta is member of the board of directors of the IEEE Industry Application Society (IAS) and Editor in Chief of the IEEE Open Journal of Industry Applications since 2020; he is IEEE-IAS Education Department chair since 2023. He has been vice-chair and Chair of the IEEE IAS Industrial Power Conversion Systems Department (2018-2021) and secretary, vice chair and Chair of the IEEE IAS Industrial Power Converters Committee (2012-2017). His research interests include control and optimization of power converters and drives, Matrix and multilevel converters.