Multiobjective Optimization of an Input-Series-Output-Parallel LLC Converter

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***Abstract*—This paper presents a systematic design methodology for input-series-output-parallel (ISOP) LLC resonant converters. A genetic algorithm (GA) is employed to optimize key design parameters, including the number of modules, switching frequency, and transformer characteristics. The optimization process simultaneously considers semiconductor and transformer power losses, as well as total transformer volume, as objective functions. The proposed approach provides a flexible design space, enabling tailored solutions based on efficiency or size constraints.**

***Index Terms*—Input-series-output-parallel (ISOP), LLC converter, isolated dc-dc converter, genetic algorithm (GA), high-frequency transformer (HFT), wide-bandgap transistors, gallium nitride (GaN).**

I. Introduction

Isolated dc-dc converters are fundamental components across diverse sectors due to their high efficiency, compact size, and galvanic isolation, which ensures safe and reliable power transfer between voltage domains [1]. They enable critical functions in medium voltage dc (MVDC) grids, such as integrating renewable energy sources, linking different voltage levels, and isolating faults to enhance system reliability [2], [3]. Similarly, data centers rely on these converters to step down the typical 400 V dc bus to 12 or 48 V [4]. In transportation, including railways, electric vehicles, and more electric aircraft, their high power density and efficiency contribute to reduced size and weight [5]–[7].

Among isolated single-input single-output dc-dc converters, two primary topology families are commonly employed: dual active bridge (DAB) converters and LLC resonant converters [8]. The DAB converter is particularly advantageous in applications requiring tight output voltage regulation, due to the wide set of modulations and control strategies available in the literature [9]. When properly designed, the DAB converter can achieve soft-switching under rated conditions, enabling zero-voltage switching (ZVS) turn-on across all the semiconductor devices. However, its soft-switching capability often deteriorates under partial load, resulting in reduced efficiency due to the loss of ZVS in one or both bridges [10]. In contrast, the LLC resonant converter, though generally less flexible in control and regulation, offers superior efficiency under light and medium load conditions, while maintaining comparable performance to the DAB at rated power levels [10].

To meet the strict requirements for high switching frequency and power density, wide-bandgap semiconductors, particularly gallium nitride (GaN) devices, are increasingly favored for power switches. Compared to silicon (Si) or silicon carbide (SiC) devices of similar voltage and current ratings, GaN transistors exhibit lower on-resistance, reduced switching losses, and better thermal performance, making them well-suited for compact, high-efficiency designs [11]. However, commercially available GaN devices are currently limited to voltage ratings up to approximately 650 V, while only a few devices are available for higher voltage ratings.

To extend the applicability of GaN devices to higher voltage levels, modular converter architectures are often employed. A commonly adopted configuration is the input-series-output-parallel (ISOP) structure, wherein multiple converter modules are connected with their inputs in series and outputs in parallel [12]. This approach is not limited to LLC converters but

is broadly applicable to isolated dc-dc converters operating in scenarios where a high input voltage must be distributed across multiple modules [13]. The ISOP configuration offers several additional advantages. In step-down applications, the high output current can be shared among multiple modules, reducing the current stress on individual devices and distributing power losses more evenly, thereby improving thermal management and overall efficiency. Furthermore, the modular nature of the ISOP architecture simplifies the design process, enables scalability to different voltage and power levels, and enhances system reliability through the potential integration of redundant modules [13].

In [14], the impact of parameter mismatches in the resonant tanks of different modules on input voltage sharing (IVS) and output current sharing (OCS) in LLC converters is investigated. An analytical model based on the first harmonic approximation (FHA) is developed to identify which parameters influence voltage and current imbalances. This analysis is extended in [15] to investigate how such mismatches affect the system's ZVS boundaries, again employing an FHA-based model with a focus on dead-time intervals. In [16], an ISOP dc-dc converter composed of series-connected LLC and buck/boost stages is studied. A detailed model is developed to quantify the input voltage deviation caused by parameter mismatches among modules.

In parallel, design-oriented studies have explored optimization strategies for resonant converters. A multiobjective optimization approach is proposed in [17] for a series-resonant dc-dc converter, where transformer volume, semiconductor, and passive component losses are optimized. More recently, [18] applies a genetic algorithm (GA) to perform multiobjective optimization of the high-frequency transformer (HFT) in an ISOP LLC converter. Different numbers of modules are considered, and Pareto fronts are used to visualize the trade-offs between efficiency and power density. However, this approach neglects semiconductor losses and assumes a fixed switching frequency, which limits the generality of the results.

This paper is structured as follows. Section II describes the topology of the ISOP LLC converter. Section III presents the methodology used to design the converter parameters. Section IV details the analytical models used to estimate power losses in GaN transistors within the LLC converter, and provides an efficiency calculation example for an ISOP LLC converter considering different numbers of modules. Section V introduces the proposed multiobjective GA-based design approach to design an ISOP LLC converter, which considers as objective functions the power losses in both the HFT and the transistors, as well as the HFT volume. Finally, Section VI concludes the paper.

II. ISOP LLC Converter Topology

Fig. 1 shows the converter topology, composed of N LLC modules connected in ISOP configuration. On the input side, a capacitive divider is used to divide the total input voltage V_{in}. All the outputs are connected in parallel to a capacitive filer C_o, before the load R_{load}.

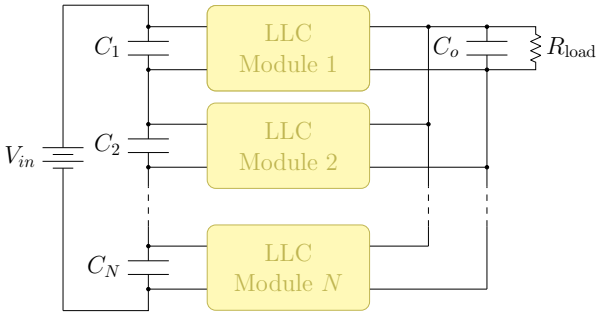

Fig. 1. Topology of the ISOP LLC converter.

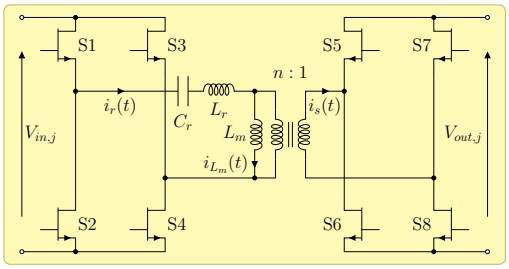

Fig. 2. LLC converter module.

Fig. 2 shows an LLC module. The high-voltage side is considered as the input stage, whereas the low-voltage side serves as the output stage. The input full-bridge is composed of GaN transistors, performing a dc-ac conversion. On the ac side, the capacitor C_r and inductor L_r compose the resonant tank. L_r and C_r define the primary resonance frequency f_r of the tank as

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

An HFT with magnetizing inductance L_m, referred to the primary side, and turns ratio n, is the key of the large voltage conversion and provides galvanic isolation between the input and the output ports. On the secondary side of the HFT, a full-bridge composed of GaN devices is considered. The output bridge implements synchronous rectification (SR) to decrease the power losses on the secondary side in comparison to a diode rectifier. The input and output voltages of the LLC modules are denoted as $V_{in,j}$ and $V_{out,j}$, respectively.

The LLC modules are assumed to be uncontrolled and to operate at resonance, i.e., with the switching frequency f_s equal to the resonant frequency f_r. Fig. 3 shows the typical waveforms in an LLC resonant converter at resonance on one switching period T_s. The top plot shows the gating signals for the eight switches. The switches S1 and S4 are commanded with square wave modulation, with duty cycle equal to 50%. S2 and S3 are commanded complementary to S1 and S4. The switches on the secondary side follow the same pattern to achieve the SR. In the middle plot, the blue line represents the current in the resonant tank $i_r(t)$, while the orange line corresponds to the magnetizing current $i_{L_m}(t)$. Due to the operation at resonance, $i_r(t)$ follows a sinusoidal behavior, while $i_{L_m}(t)$ is a triangular waveform, due to the voltage

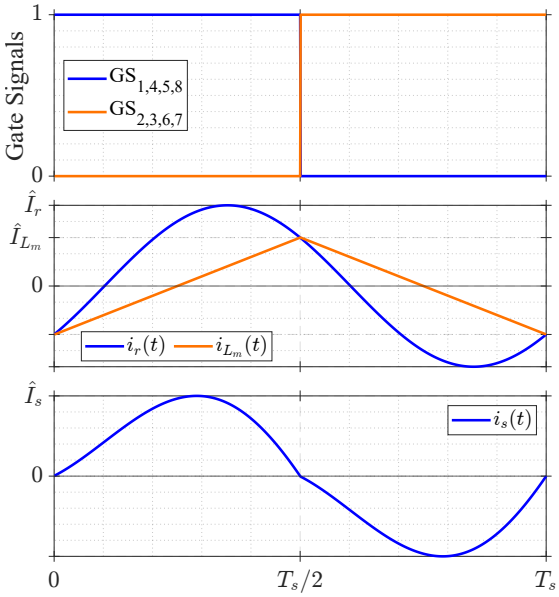

Fig. 3. Waveforms in an LLC converter. (Top) Gate signals for the switches S1, S4, S5 and S8 in blue, and for S2, S3, S6 and S7 in orange. (Middle) Resonant tank current in orange, and magnetizing current in blue. (Bottom) Current on the secondary side of the HFT.

applied to L_m being a square waveform. Finally, the bottom plot shows the current on the secondary side of the HFT $i_s(t)$, resulting as

$$i_s(t) = n\big(i_r(t) - i_{L_m}(t)\big) \tag{2}$$

For the evaluation of power losses, the peak magnetizing current $\hat{I}_{L_m}$, as well as the RMS values of the resonant tank current I_r and the secondary-side current of the HFT I_s, can be obtained as follows [19]

$$\hat{I}_{L_m} = \frac{nV_{out,j}}{4L_m f_s} \tag{3}$$

$$I_r = \sqrt{\frac{\pi^2 P_{out,j}^2}{8V_{in,j}^2} + \frac{1}{2}\hat{I}_{L_m}^2} \tag{4}$$

$$I_s = n\sqrt{I_r^2 + \left(\frac{1}{3} - \frac{8}{\pi^2}\right)\hat{I}_{L_m}^2} \tag{5}$$

where $P_{out,j}$ is the output power of the LLC module.

III. Design of the LLC Modules

Table I reports the specifications of the ISOP LLC converter adopted in this work, where $V_{in,n}$ and $V_{out,n}$ represent the nominal input and output voltages, respectively, $P_{out,n}$ denotes the nominal output power, and T_{dt} refers to the modulation dead time. Assuming no parameter mismatches in the LLC modules, the modules achieve perfect IVS. Therefore, the input voltage on each module is equal to

$$V_{in,j} = \frac{V_{in}}{N} \tag{6}$$

When the LLC operates at resonance, the converter behaves as a dc transformer (DCX), and the output voltage depends

TABLE I
Specifications of the ISOP LLC converter

Parameter	Value
$V_{in,n}$	800 V
$V_{out,n}$	36.36 V
$P_{out,n}$	2.5 kW
Input voltage range	600–1000 V
T_{dt}	62.5 ns

solely on the input voltage and the turns ratio of the HFT, as defined in

$$V_{out,j} = \frac{V_{in,j}}{n} \tag{7}$$

Thus, n is determined from the nominal voltage values.

Based on the rated voltage requirements and an initial estimation of the transistor currents, suitable GaN transistors can be selected. The transistor output capacitance C_{oss} as a function of the drain-source voltage v_{DS} can be obtained from the datasheets and used to calculate the charge-equivalent output capacitance function $C_{\text{oss,q}}$, defined as [20]

$$C_{\text{oss,q}}(v_{\text{DS}}) = \frac{1}{v_{\text{DS}}}\int_0^{v_{\text{DS}}} C_{\text{oss}}(v)\,dv \tag{8}$$

Defining $C_{\text{oss,q,HV}}$ and $C_{\text{oss,q,LV}}$ the charge-equivalent output capacitances of the transistors on the input and output sides, respectively, it is possible to refer $C_{\text{oss,q,LV}}$ to the input side, and define an equivalent capacitance C_{eq} as

$$C_{\text{eq}} = m_{\text{HV}}C_{\text{oss,q,HV}} + \frac{m_{\text{LV}}C_{\text{oss,q,LV}}}{n^2} \tag{9}$$

where m_{HV} and m_{LV} refer to the number of parallel transistors for each switch on the input and output sides, respectively.

The condition to ensure the ZVS turn-on in the LLC converter, assuming i_{L_m} remains constant during the dead-time, and equal to its peak value $\hat{I}_{L_m}$, is obtained as [21]

$$L_m \leq \frac{T_{dt}}{8f_s C_{\text{eq}}} \tag{10}$$

Next, L_r and C_r have to be defined. L_r is typically derived from the leakage inductance of the HFT, referred to the primary side. To achieve good IVS despite slight parameter mismatches, the ratio L_r/L_m should be kept small [15], [16]. In this work, a value of $L_r/L_m = 0.1$ is considered. Subsequently, C_r is defined according to L_r and f_r as in (1). Finally, $\hat{I}_{L_m}$, I_r, and I_s are calculated with (3)–(5).

IV. Power Losses in GaN Transistors

In GaN transistors, four categories of power losses can occur: conduction losses P_{cond}, switching losses P_{sw}, gate charge losses P_{G}, and reverse conduction losses P_{SD} [22].

When a transistor is turned on, and a current flows from drain to source, the internal on-resistance of the device causes conduction losses. Therefore, the transistor conduction loss on each device can be calculated as

$$P_{\text{cond}} = \frac{1}{2}\frac{R_{\text{DS(on)}}}{m}I_{\text{RMS}}^2 \tag{11}$$

TABLE II
CONFIGURATIONS OF THE ISOP LLC CONVERTER

Configuration	N	HV devices	m_{HV}	LV devices	m_{LV}	L_m [μH]	L_r [μH]	C_r [nF]	$I_{r,\text{max}}$ [A]	$I_{s,\text{max}}$ [A]
1	1	GPIXV30DFN	1	EPC2302	3	116.45	11.64	13.60	5.16	102.38
2	2	GS-065-030-2-L	1	EPC2306	3	90.93	9.09	17.41	4.69	50.94
3	6	EPC2215	1	EPC2306	1	24.93	2.49	63.50	4.64	16.97
4	8	GAN7R0-150LBE	1	EPC2306	1	30.66	3.07	51.63	4.63	12.73
5	12	EPC2204	1	EPC2204	1	28.25	2.83	56.03	4.63	8.48

where $R_{\text{DS(on)}}$ refers to the on-resistance of the input or output side transistors, m is the number of parallel devices for each switch, and I_{RMS} is the RMS of the currents $i_r(t)$ or $i_s(t)$.

Switching losses consist of turn-on and turn-off losses, denoted as $P_{\text{sw,on}}$ and $P_{\text{sw,off}}$, respectively. When the LLC converter is designed to achieve ZVS at turn-on, its turn-on losses are eliminated in both the input and output bridges. However, the input-side switches operate under hard-switching conditions during turn-off. As shown in Fig. 3, the current flowing through the input-side bridge at turn-off is $\hat{I}_{L_m}$. Accordingly, the turn-off losses for each input-side switch can be calculated as

$$P_{\text{sw,off}} = \frac{1}{m_{\text{HV}}} \frac{1}{12} \frac{\left(\hat{I}_{L_m} t_{\text{cf}}\right)^2}{C_{\text{oss}}(0) + C_{\text{oss}}(V_{in,j})} f_s \tag{12}$$

where t_{cf} is the current fall time, as described in [22]. In contrast, Fig. 3 shows that the output-bridge current is zero at turn-off. As a result, the output bridge achieves zero-current switching (ZCS) during turn-off, resulting in zero turn-off losses.

Gate-charge losses result from the charge Q_{G} required to switch the devices on and off. This charge is accumulated on the gate and dissipated once per switching cycle. For each device, the gate-charge losses are calculated as

$$P_{\text{G}} = Q_{\text{G}}(V_{\text{G(on)}} - V_{\text{G(off)}}) f_s \tag{13}$$

where $V_{\text{G(on)}}$ and $V_{\text{G(off)}}$ are the voltages to turn on and off the transistor, respectively.

Finally, reverse conduction losses are characteristic of GaN transistors and occur when the device is off but a current flows from source to drain. Therefore, the device behaves like a freewheeling diode, resulting in a source-drain voltage drop V_{SD}, which is specified in the datasheet as a function of the source-drain current I_{SD}. Then, P_{SD} is calculated as

$$P_{\text{SD}} = I_{\text{SD}} V_{\text{SD}} t_{\text{SD}} f_s \tag{14}$$

where t_{SD} is the reverse conduction time, whose calculation is explained in [22].

A. GaN power losses calculation in the ISOP LLC converter

An example of the calculation of the power losses of an ISOP LLC converter is reported here, considering $f_s = 400$ kHz. Based on the converter specifications provided in Table I, and considering the GaN transistors available on the market at the time of the work, the converter can be designed in five different configurations, summarized in Table II. L_m is calculated as the upper limit of (10) considering the worst-case scenario, i.e. when the input voltage is minimum and, as a consequence, C_{eq} is maximum. $I_{r,\text{max}}$, and $I_{s,\text{max}}$ are the maximum values for I_r and I_s, occurring when the output power is maximum and the input voltage is minimum.

The transistor power losses are computed for each configuration over a range of operating conditions. Specifically, both the input voltage and output power ranges are discretized into 150 sub-intervals each, resulting in a grid of 150^2 points of operation. In each point, (11)–(14) are used to evaluate the power losses, and the efficiency η is calculated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{GaN}}} \tag{15}$$

where P_{GaN} is defined as

$$P_{\text{GaN}} = P_{\text{cond}} + P_{\text{sw}} + P_{\text{G}} + P_{\text{SD}} \tag{16}$$

The results of the efficiency calculation are reported in Fig. 4, where the efficiency is pictured using a scale of colors in the V_{in}–P_{out} plane. Specifically, Fig. 4a, 4b, 4c, 4d, and 4e report the efficiency results corresponding to the configurations 1, 2, 3, 4, and 5, respectively. According to the results, a higher number of modules causes an enhancement in the efficiency of the converter when considering the power losses solely in the transistors. This is caused by the better characteristics and performances of low voltage GaN transistors with respect to the higher voltage ones.

V. MULTIOBJECTIVE OPTIMIZATION OF ISOP LLC CONVERTER

An increase in the number of modules leads to a reduction in transistor power losses; however, regarding the HFT, a greater number of modules enhances power density while adversely affecting power losses [17], [18]. Therefore, designing an ISOP LLC converter requires solving a multiobjective optimization problem.

In this work, a GA-based multiobjective optimization is performed, selecting the power losses in the transistors P_{GaN}, the HFT power losses P_{HFT} and volume V_{HFT} as objective functions. The objectives P_{GaN} and P_{HFT} are decoupled to enhance population diversity within the GA. For each individual in the population, the HFT turns ratio and resonant tank parameters are designed based on that individual's optimization variables. Then, the transformer core and the litz-wire windings are selected from two databases. Specifically, the core database was derived from the TDK catalogue, considering three different

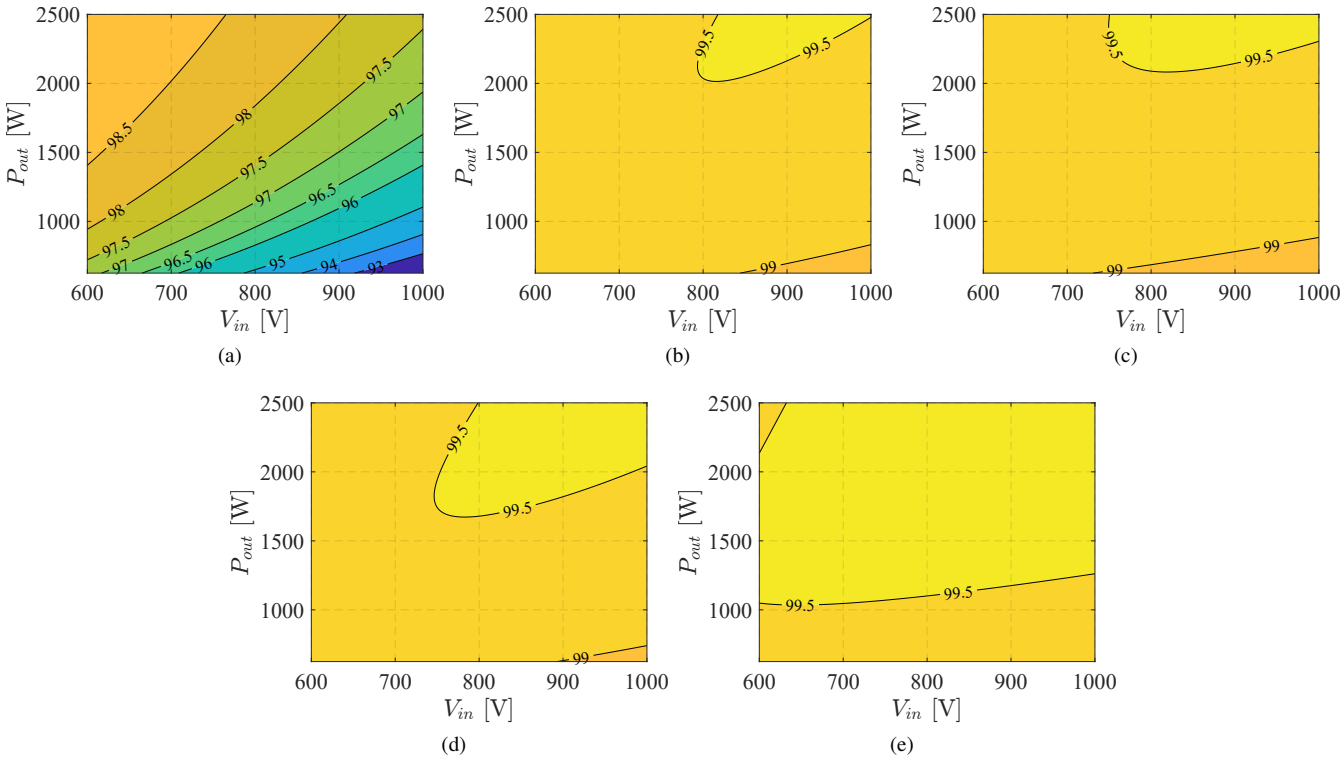

Fig. 4. Efficiency results for the ISOP LLC converter for $f_s = 400$ kHz and in five different configurations. (a) Configuration 1 ($N = 1$). (b) Configuration 2 ($N = 2$). (c) Configuration 3 ($N = 6$). (d) Configuration 4 ($N = 8$). (e) Configuration 5 ($N = 12$).

core geometries—EE, PQ, and ETD —and twenty different ferrite materials, i.e., PC47, PC90, PC95, PC40, PE22, PEL95, PEM95, PC50, PCT50, PC200, N27, N87, N88, N95, N96, N97, N49, N41, N72, N92. Finally, the objective functions are evaluated, multiplying P_{HFT}, P_{GaN}, and V_{HFT} by the considerd number of modules N, and a new population is set according to the best individuals of the population at the previous step.

Specifically, the optimization variables selected are the peak flux density in the HFT core B_{PK}, the window utilization factor k_u [23], the core shape n_{CS}, the core material n_{CM}, the number of modules of the ISOP converter N, and the switching frequency f_s. B_{PK} is constrained to be between 50 and 400 mT, to prevent core saturation. The limits for k_u are set between 0.2 and 0.45, according to the typical values from the literature. n_{CS} and n_{CM} are integer numbers to select one of the three considered core shapes and one of the twenty ferrite materials, respectively. N is an integer number, whose five different values were reported in Table II. Finally, f_s was limited between 200 kHz and 1 MHz.

When the algorithm starts, if an individual's core shape or switching frequency is incompatible with its selected ferrite material, the individual is immediately penalized by assigning a value of 10^6 to all its objective functions. Otherwise, the tank parameters are designed following the procedure shown in the previous section. Then, P_{GaN} is calculated in the worst-case scenario for the converter, namely $V_{in} = V_{in,\text{min}}$ and $P_{out} = P_{out,n}$, using (11)–(14).

Subsequently, the optimal core-geometry factor model (OKGM) approach described in [24] has been employed to select a specific core and litz-wire from the databases, and to size the core airgap g_c, the number of primary N_p and secondary turns N_s, and an estimation of the magnetizing inductance $\hat{L}_m$. Then, the core volume V_{c} and the winding volume V_{w} are added to calculate V_{HFT}.

Finally, P_{HFT} is calculated as the sum of the core losses P_{c} and the winding losses P_{w}. P_{c} is calculated using the waveform coefficient Steinmetz equation (WcSE) [25]

$$P_{\text{c}} = \frac{\pi}{4} K_{\text{SE}} f^{\alpha_{\text{SE}}} B_{\text{PK}}^{\beta_{\text{SE}}} V_{\text{c}} \tag{17}$$

where K_{SE}, α_{SE} and β_{SE} are the Steinmetz coefficients of the materials, and are obtained by fitting the experimental losses, reported in the ferrite datasheets, as functions of the peak flux density and the excitation frequency f, here corresponding to the switching frequency. P_{w} is calculated using

$$P_{\text{w}} = \frac{F_{\text{R}} \rho_{\text{w}} V_{\text{w}} \Sigma\text{VA}^2}{k_u K_{\text{wf}}^2 f^2 B_{\text{PK}}^2 A_{\text{c}}^2 A_{\text{w}}^2} \tag{18}$$

where F_{R} is a factor which takes into account the high-frequency effects, ρ_{w} is the copper electrical resistivity, ΣVA is the voltampere rating of the transformer, K_{wf} is the voltage waveform factor—equal to 4.0 for square waveforms—and A_{c} and A_{w} are the core and window areas, respectively.

Following the assignment of the objective function values, three constraint conditions are checked. If any of the three constraints is violated, the individual is penalized assigning

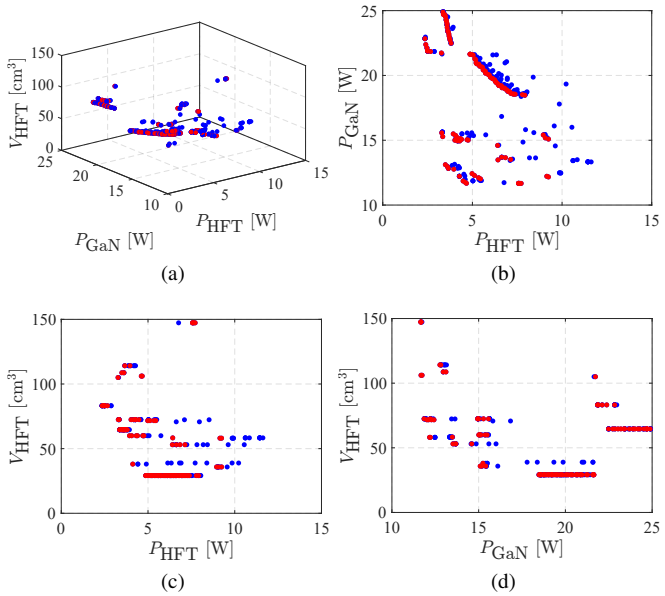

Fig. 5. Multiobjective optimization results of the ISOP LLC converter. The red points correspond to the optimal solutions, while the blue points are the suboptimal population. (a) 3-D plot of the results. (b) Projections on the P_{HFT}–P_{GaN} plane. (c) Projections on the P_{HFT}–V_{HFT} plane. (d) Projections on the P_{GaN}–V_{HFT} plane.

the value 10^6 to its objective functions. The first condition regards the estimated temperature rise ΔT_{rise}. For a transformer without an external cooling system, dissipating heat through thermal radiation and convection to the surrounding air, the temperature rise ΔT_{rise} is calculated as [23]

$$\Delta T_{\mathrm{rise}} = 450\left(\frac{P_{\mathrm{HFT}}}{A_{\mathrm{surf}} \cdot 10^4}\right)^{0.826} \tag{19}$$

where A_{surf} is the total surface area of the HFT. ΔT_{rise} must be below a certain threshold, here set equal to 50 °C, otherwise the individual is penalized. The second condition is a geometrical constraint. In the GA, the dimensions of the windings are compared with the window ones. If one of the winding dimensions is larger than the corresponding one of the window, the individual is penalized. Finally, if the absolute error between the estimated magnetizing inductance $\hat{L}_m$ and the designed value is larger than a certain threshold, here set equal to 2%, the individual is penalized.

A. Multiobjective optimization results

The proposed multiobjective optimization has been implemented using the gamultiobj function from the Global Optimization Toolbox in MATLAB R2023a. The population size of each generation has been set to 300, as the maximum number of generations.

Fig. 5 shows the results of the optimization. Specifically, Fig. 5a shows the results on a 3-D Pareto front. The red points correspond to the Pareto optimal solutions, while the blue points are the suboptimal population. Fig. 5b, 5c and 5d show the projections of the optimization results on the P_{HFT}–P_{GaN}, P_{HFT}–V_{HFT}, and P_{GaN}–V_{HFT} planes, respectively.

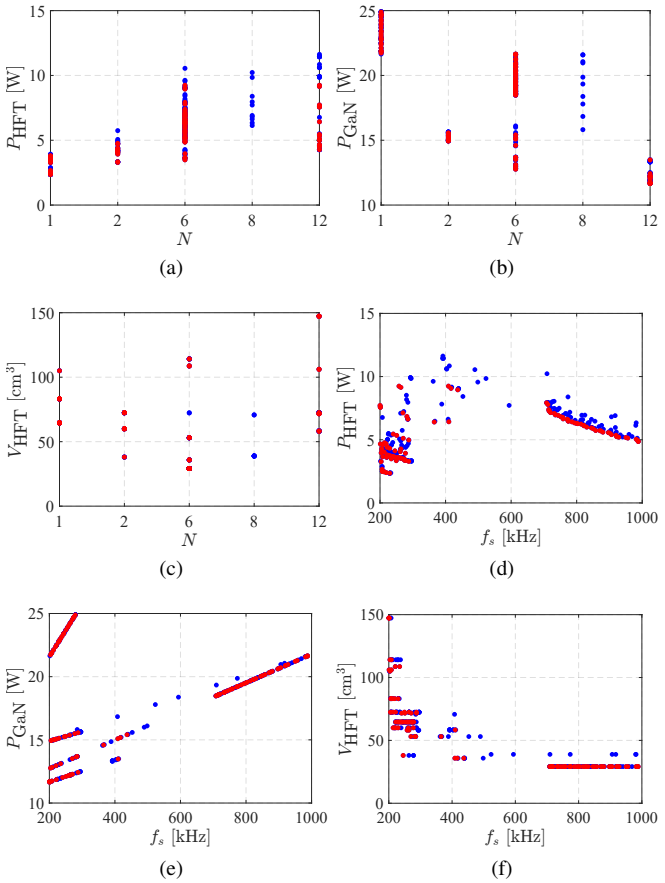

Fig. 6. Effect of N and f_s on the objective functions. The red points correspond to the optimal solutions, while the blue points are the suboptimal population. (a) Effect of N on P_{HFT}. (b) Effect of N on P_{GaN}. (c) Effect of N on V_{HFT}. (d) Effect of f_s on P_{HFT}. (e) Effect of f_s on P_{GaN}. (f) Effect of f_s on V_{HFT}.

TABLE III
OPTIMAL SOLUTIONS

Parameter	$P_{\mathrm{HFT,min}}$	$P_{\mathrm{GaN,min}}$	$V_{\mathrm{HFT,min}}$
P_{HFT} [W]	2.35	7.72	4.87
P_{GaN} [W]	22.84	11.67	21.64
V_{HFT} [cm^3]	83.19	147.31	29.16
B_{PK} [mT]	52	50	51
k_u	0.29	0.20	0.20
n_{CS}	3 (EE)	3 (EE)	2 (PQ)
n_{CM}	1 (PC47)	1 (PC47)	17 (N49)
N	1	12	6
f_s [kHz]	229.97	200.17	987.83

The minimum power losses in the HFT and in the semiconductor devices are 2.35 W and 11.67 W, respectively, while the minimum volume that can be reached is 29.16 cm^3. The solutions with minimum objective functions and their optimization variables are summarized in Table III.

Finally, Fig. 6 shows the relation between two optimization variables, N and f_s, with the objective functions. Fig. 6a and 6b show that for a higher number of modules, the power losses in the HFT increase, while the power losses in the transistors

decrease, in accordance with Fig. 4. Fig. 6c reveals that, while increasing the number of modules from 1 is beneficial for decreasing the HFT volume, a further increase after $N = 6$ will produce the opposite effect. Finally, as expected, higher switching frequencies cause an increment in both power losses and a decrease in the HFT volume, as shown in Fig. 6d, 6e and 6f, respectively.

VI. Conclusion

Conventional LLC converters are typically designed in an ISOP configuration for applications where high voltage or high power levels preclude the use of GaN transistors, which are currently optimized for low voltage ratings. When considering only transistor power losses, increasing the number of modules improves converter efficiency; however, this generally leads to higher power losses in the HFT.

This paper presented a multiobjective optimization of an ISOP LLC converter using a GA approach, with the objective functions being the power losses in the HFT, the power losses in the transistors, and the volume of the HFT. The optimization variables include peak flux density, window utilization factor, core shape and material, number of modules, and switching frequency. The proposed methodology enables the identification of optimal tradeoffs between efficiency and size, offering designers a flexible design space to accommodate a wide range of application requirements.

Acknowledgment

This work was supported by the Marie Skłodowska-Curie Actions (MSCA) under the European Union's Horizon 2020 Research and Innovation Staff Exchange (RISE) under Grant 872001.

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