Performance Assessment of ISOP LLC with Buck-Boost Post-Regulator and ISOP LLC-DAB

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***Abstract*—This paper provides a comparative efficiency analysis of two dc-dc topologies — LLC with non-inverting buck-boost post-regulator and LLC-DAB—by evaluating the losses of Gallium Nitride (GaN) HEMTs in both converter topologies. The study considers conduction, switching, gate driver, and reverse conduction losses to ensure a comprehensive comparison. Results demonstrate that the LLC-DAB topology achieves superior efficiency, particularly at full power, due to the Zero-Voltage Switching (ZVS) capability of the DAB stage, which minimizes switching losses and enhances the performance of the LLC modules. In contrast, the LLC with non-inverting buck-boost post-regulator topology exhibits higher efficiency at lower power levels but suffers from increased switching losses at full load due to its hard-switching operation.**

***Index Terms*—DAB converter, efficiency comparison, LLC converter, LLC-DAB, non-inverting, buck-boost, Input-Series-Output-Parallel, GaN HEMTs.**

I. Introduction

The rapid progress of renewable energy systems, electric vehicles, and energy storage solutions has made an efficient isolated dc–dc converter essential for managing bidirectional power flow [1]–[3]. High-power isolated DC-DC converters are essential for connecting DC grids with different voltage levels, where efficiency and controllability are critical for optimal performance. Among various converter topologies, the Dual Active Bridge (DAB) and LLC resonant converters stand out due to their advantages in power control, high efficiency and power density [4]–[7]. The DAB converter offers high controllability and bidirectional power transfer with the potential for soft-switching operations, i.e., Zero-Voltage Switching (ZVS). However, its efficiency can be limited by turn-off losses of semiconductor devices. The LLC resonant converter, when operating at its resonant frequency, achieves very high efficiencies and wide ZVS ranges [5]. However, it often suffers from limited output voltage regulation capability.

To facilitate the use of commercially available power devices in high-voltage applications, modular converter topologies are often employed. These structures enable the use of advanced power semiconductor technologies, such as Gallium Nitride (GaN) HEMTs, which exhibit lower on-resistance, higher achievable switching frequencies, and improved thermal performance compared to Silicon (Si) and Silicon Carbide (SiC) devices. However, HV GaN devices remain relatively new to the market, with 1200 V GaN technology still not widely adopted.

A common modular implementation is the Input-Series-Output-Parallel (ISOP) configuration, particularly with the LLC converter [8]. This approach allows the use of more mature LV GaN devices, which offer a superior Figure-of-Merit (FOM) and enhance overall converter efficiency and performance. Additionally, the ISOP configuration distributes the high secondary current among multiple modules, reducing thermal stress on power devices and transformers [9].

However, modular structures based solely on LLC converters present challenges in voltage regulation. Typically, LLC converters operate in an open-loop configuration with a fixed switching frequency tuned to their resonance frequency, maximizing efficiency by functioning as a DC Transformer (DCX) [10]. While this approach minimizes losses, it limits voltage control flexibility. Two strategies are usually adopted to address this issue:

1) Post-regulation using a buck, boost or buck-boost converter, placed in series with the ISOP converter [11].
2) Hybrid regulation with a DAB converter in ISOP connection with the LLC converter, that combine the strengths of DAB and LLC converters. The LLC converter is primarily operating as a high-efficiency DCX, transferring the majority of the power. The DAB converter is used in parallel or series-parallel to regulate the output voltage [12].

Several works have explored both approaches to enhance efficiency, controllability and power density. The post-regulation

approach is adopted in [13], where an ISOP system integrating a non-isolated pre- or post-regulator (buck or boost) is proposed. This topology naturally achieves Input-Voltage Sharing (IVS) and Output-Current Sharing (OCS) through a common duty ratio while maximizing efficiency at a fixed switching frequency slightly below resonance. Similarly, [14] employs a two-stage structure where a CLLC resonant converter operates at a fixed conversion ratio, followed by a buck post-regulator for voltage control. This separation of power transfer and regulation improves efficiency, achieving over 98% efficiency by reducing voltage stress on the post-regulator switches. The LLC-DAB approach is explained in [15], where a bidirectional DCX topology to enhance both efficiency and regulation is introduced. By connecting the LLC and DAB converters in series at the input and in parallel at the output, the system ensures high-efficiency power transfer through the LLC stage while utilizing the DAB stage for dynamic voltage regulation. Additionally, the DAB converter extends the ZVS range and supports bidirectional power flow, making this topology suitable for applications requiring energy recovery. In [16], a hybrid ISOP approach that combines Series Resonant Converters (SRCs) for bulk power transfer with DAB converters for partial power regulation is explored. By processing most of the power through SRCs while using DABs for voltage control, this strategy achieves a balance between efficiency, reduced complexity, and enhanced load adaptability.

Finally, both approaches are employed to ensure voltage regulation and achieve high efficiency. However, no direct comparison has been conducted to date. Therefore, this paper addresses this gap by analytically evaluating both solutions in terms of efficiency to determine which is more suitable under specific operating conditions. To ensure a consistent comparison and assess the latest advancements in device technology, GaN HEMTs have been implemented across all fundamental converters (LLC, DAB, and buck-boost) in both topologies. The analysis considers all key sources of losses conduction, switching, gate driver, and reverse conduction losses, providing a comprehensive framework for evaluating the performance of each solution. This paper is organized as follows. Section II shows the two topologies under comparison, namely the ISOP LLC with non-inverting buck-boost post-regulator and the ISOP LLC-DAB, and treats analytically the operations of each conversion stage. Section III details the semiconductor power losses considered for both topologies. Specifically, the equations for the conduction, switching, reverse conduction, and gate charge losses in the GaN HEMTs are presented. Section IV presents the efficiency comparison between the two topologies, giving the details of the impact of each type of losses. Section V concludes the paper.

II. Topologies under comparison

The circuit topologies analyzed in this study are illustrated in Fig. 1. Specifically, Fig. 1a presents the ISOP LLC topology with a non-inverting buck-boost post-regulator, while Fig. 1b depicts the ISOP LLC-DAB configuration. The parameters for both topologies are listed in Table I. The following sections provide a detailed explanation of each converter: LLC, non-inverting buck-boost, and DAB.

TABLE I: System parameters.

Parameter	Value
Rated power P	2 kW
Input voltage (range) V_{in}	600–1000 V
Nominal input voltage $V_{in,\text{nom}}$	800 V
Nominal output voltage $V_{out,\text{nom}}$	48 V
Switching frequency f_s	400 kHz
Dead-time T_{dt}	62 ns

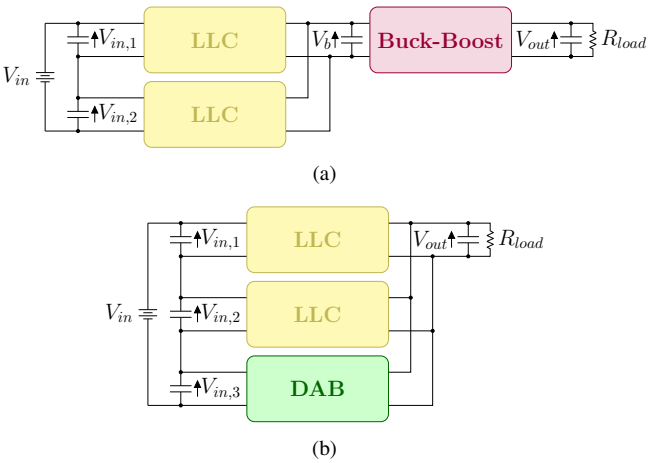


Fig. 1: Converters investigated in this analysis. (a) Two LLC modules in ISOP configuration, and a non-inverting buck-boost post-regulator. (b) Two LLC modules and a DAB in ISOP configuration.

A. Model of the LLC converter

Fig. 2 shows the topology of the LLC converter adopted in this work. Both the input and the output sides consist of full bridges, connected with a High Frequency Transformer (HFT) and an LC resonant tank. The switches on the output bridge work as a synchronous rectifier to increase the efficiency compared to a conventional diode bridge rectifier.

The HFT turns ratio is designed according to the nominal input and output voltages, $V_{in,\text{nom,LLC}}$ and $V_{out,\text{nom,LLC}}$, respec-

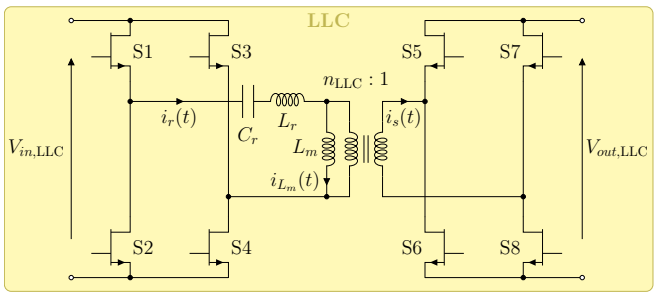


Fig. 2: LLC converter topology.

tively, as:

$$n_{\text{LLC}} = \frac{V_{in,\text{nom,LLC}}}{V_{out,\text{nom,LLC}}} \tag{1}$$

The resonant inductor L_r and capacitor C_r define the resonant frequency of the tank, according to

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

The magnetizing inductance of the transformer L_m determines the ZVS operations of the converter, as detailed in [17], [18]. This condition is expressed as:

$$L_m \leq \frac{T_{dt}}{8 f_s C_{\text{eq}}} \tag{3}$$

where T_{dt} is the modulator dead-time and C_{eq} is the charge-equivalent output capacitance of all devices. The latter is expressed as (4), and it takes into account both the charge-equivalent output capacitance of the devices on the HV side $C_{\text{oss,q,eq,HV}}$ and on the LV side $C_{\text{oss,q,eq,HV}}$ referred to the primary side of the transformer.

$$C_{\text{eq}} = C_{\text{oss,q,eq,HV}} + \frac{C_{\text{oss,q,eq,LV}}}{n_{\text{LLC}}^2} \tag{4}$$

$C_{\text{oss,q,eq,HV}}$ is defined as:

$$C_{\text{oss,q,eq,HV}}(V_{in,\text{LLC}}) = \frac{1}{V_{in,\text{LLC}}} \int_0^{V_{in,\text{LLC}}} C_{\text{oss}}(v_{\text{DS}})\, dv_{\text{DS}} \tag{5}$$

where C_{oss} is the output capacitance of the device, specified in the datasheets as a function of v_{DS}. The definition of $C_{\text{oss,q,eq,LV}}$ is analogous to (5).

The resonant inductance L_r is typically derived from the transformer's leakage inductance L_m referenced to the primary side. In an ISOP LLC, the ratio L_m/L_r is related to the maximum input voltage mismatch [13]. A typical design choice is as follows:

$$L_r = \frac{L_m}{10} \tag{6}$$

Finally, the resonant capacitance is calculated from the resonant frequency definition (2).

When the LLC operates at resonance, functioning as a DCX, the general relationship between the input and output voltage is given by:

$$V_{out,\text{LLC}} = \frac{V_{in,\text{LLC}}}{n_{\text{LLC}}} \tag{7}$$

Fig. 3 shows the typical waveforms in a switching period T_s for the LLC converter. The adopted modulation is a 50% duty-cycle square wave. The switches on the synchronous rectifier follow the same switching pattern as the switches on the input bridge. The voltage applied to L_m is a square-wave, therefore the magnetizing current $i_{L_m}(t)$ has a triangular shape. The peak of the magnetizing current $\hat{I}_{L_m}$ is used to calculate the switching losses, and is obtained by (8).

$$\hat{I}_{L_m} = \frac{n_{\text{LLC}} V_{out,\text{LLC}}}{4 L_m f_s} \tag{8}$$

where f_s is the switching frequency. The RMS values of the currents on the primary and secondary sides of the transformer,

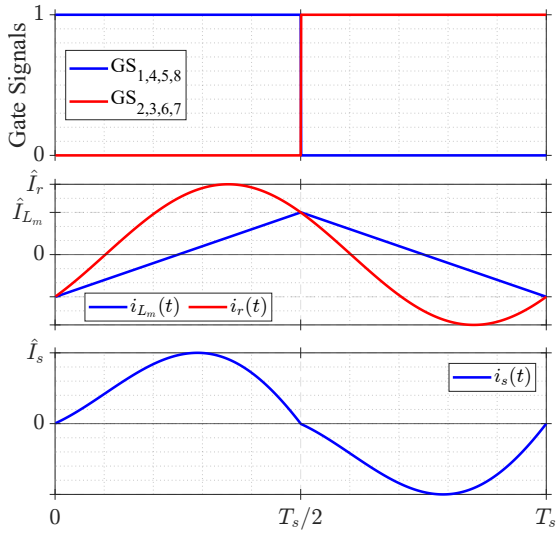


Fig. 3: Waveforms of the LLC converter. (Top) Gate signals for the switches S1, S4, S5 and S8 in blue, and for S2, S3, S6 and S7 in red. (Middle) Magnetizing current in blue, and resonant tank current in red. (Bottom) Transformer current on the secondary side.

I_r and I_s, respectively, are required to calculate the conduction losses in the HEMTs. Given the converter's output power $P_{out,\text{LLC}}$, I_r and I_s can be computed using the condition in (9), resulting in the expressions in (10) and (11) [19].

$$\frac{2}{T_s} \int_0^{\frac{T_s}{2}} i_s(t)\, dt = \frac{P_{out,\text{LLC}}}{V_{out,\text{LLC}}} \tag{9}$$

$$I_r = \sqrt{\frac{\pi^2 P_{out,\text{LLC}}^2}{8 n_{\text{LLC}}^2 V_{out,\text{LLC}}^2} + \frac{1}{2}\hat{I}_{L_m}^2} \tag{10}$$

$$I_s = n_{\text{LLC}} \sqrt{I_r^2 + \left(\frac{1}{3} - \frac{8}{\pi^2}\right)\hat{I}_{L_m}^2} \tag{11}$$

B. Model of the non-inverting buck-boost converter

Fig. 4 shows the topology of the non-inverting buck-boost, consisting in two half-bridges connected by an inductance L_{BB} on their ac midpoint terminals. The switches S1 and S4 are commanded by using a Pulse Width Modulation (PWM), while S2 and S3 are set in the complementary state. The duty cycle D defines the relationship between the output and input voltages, according to

$$V_{out,\text{BB}} = \frac{D}{1-D} V_{in,\text{BB}} \tag{12}$$

Fig. 5 shows the gate signals of the four switches in the top figure, while the inductor current $i_{L_{\text{BB}}}(t)$ is shown in the bottom figure. $i_{L_{\text{BB}}}(t)$ consists of a dc component $\overline{I_{L_{\text{BB}}}}$ and a ripple $\Delta i_{L_{\text{BB}}}$, calculated as in (13) and (14), respectively.

$$\overline{I_{L_{\text{BB}}}} = \frac{P_{out,\text{BB}}}{D V_{in,\text{BB}}} \tag{13}$$

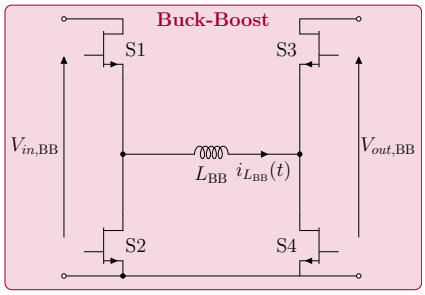


Fig. 4: Non-inverting buck-boost converter topology.

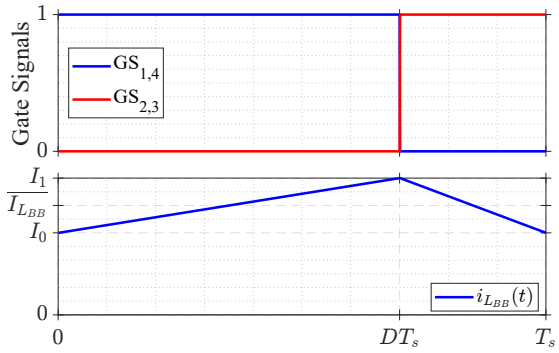


Fig. 5: Waveforms of the non-inverting buck-boost converter. (Top) Gate signals for the switches S1 and S4 in blue, and for S2 and S3 in red. (Bottom) Current in the inductance L_{BB}.

$$\Delta i_{L_{\mathrm{BB}}} = \frac{V_{in,\mathrm{BB}}}{2L_{\mathrm{BB}}} DT_s \tag{14}$$

While $\overline{I_{L_{\mathrm{BB}}}} \pm \Delta i_{L_{\mathrm{BB}}}$ is adopted for the calculation of the switching losses, the RMS value of the current $I_{L_{\mathrm{BB}}}$ is required for the conduction losses, and it is calculated as:

$$I_{L_{\mathrm{BB}}} = \sqrt{\overline{I_{L_{\mathrm{BB}}}}^2 + \frac{\Delta i_{L_{\mathrm{BB}}}^2}{3}} \tag{15}$$

C. Model of the DAB converter

Fig. 6 shows the DAB converter topology, consisting in two full bridges, connected with an inductor L_{DAB} and a transformer. Single Phase Shift (SPS) modulation is used to define the switching patterns of the 8 switches. The switches of each half-bridge are controlled to operate in a complementary state. The phase shift φ determines the transformer current

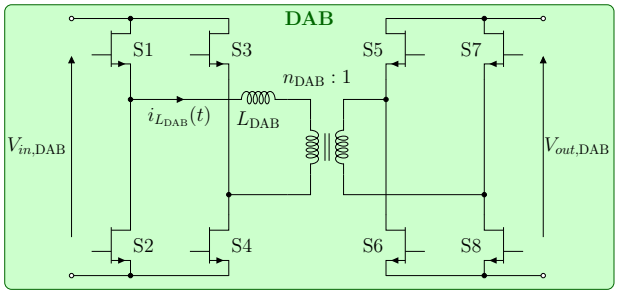


Fig. 6: DAB converter topology.

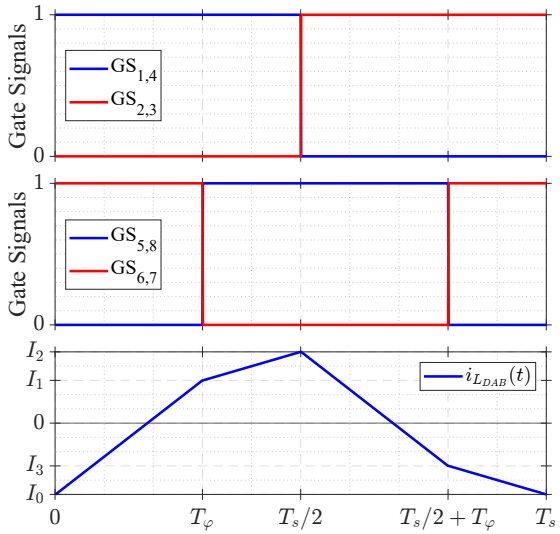


Fig. 7: Waveforms of the DAB converter. (Top) Gate signals for the switches S1 and S4 in blue, and for S2 and S3 in red. (Middle) Gate signals for the switches S5 and S8 in blue, and for S6 and S7 in red. (Bottom) Transformer current.

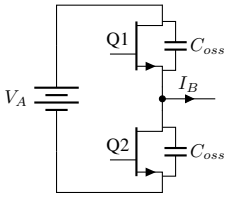


Fig. 8: GaN half-bridge, used as reference for power losses calculation.

$i_{L_{\mathrm{DAB}}}(t)$ and consequently, the amount of transferred power. Fig. 7 shows the gate signals of the two H-bridges and the corresponding transformer current. Given the required output power $P_{out,\mathrm{DAB}}$, the output voltage can be calculated as:

$$V_{out,\mathrm{DAB}} = \frac{2\pi^2 L_{\mathrm{DAB}} f_s P_{out,\mathrm{DAB}}}{n_{\mathrm{DAB}} V_{in,\mathrm{DAB}} \varphi(\pi - \varphi)} \tag{16}$$

The switching losses are evaluated by calculating the values of the current in the transformer for each switching event. Referring to Fig. 7 and denoting I_0 and I_1 the current values when S_1 and S_4, or analogously S_5 and S_8, are switching, they can be calculated using (17) and (18), respectively. I_2 and I_3 can be determined by symmetry.

$$I_0 = \frac{\pi(n_{\mathrm{DAB}} V_{out,\mathrm{DAB}} - V_{in,\mathrm{DAB}}) - 2\varphi n_{\mathrm{DAB}} V_{out,\mathrm{DAB}}}{4\pi L_{\mathrm{DAB}} f_s} \tag{17}$$

$$I_1 = \frac{\pi(n_{\mathrm{DAB}} V_{out,\mathrm{DAB}} - V_{in,\mathrm{DAB}}) + 2\varphi V_{in,\mathrm{DAB}}}{4\pi L_{\mathrm{DAB}} f_s} \tag{18}$$

Finally, the conduction losses are calculated considering the RMS value of the transformer current:

$$I_L = \frac{\sqrt{3\pi}}{12\pi^2 L_{\mathrm{DAB}} f_s} \Big[\pi^3 (V_{in,\mathrm{DAB}} - n_{\mathrm{DAB}} V_{out,\mathrm{DAB}})^2 - 4 n_{\mathrm{DAB}} V_{in,\mathrm{DAB}} V_{out,\mathrm{DAB}} \varphi^2 (2\varphi - 3\pi)\Big]^{1/2} \tag{19}$$

TABLE II: Parameters of the ISOP LLC with non-inverting buck-boost post-regulator.

Parameter	Value
LLC HV HEMTs	IGLD60R070D1
LLC LV HEMTs	EPC2088
n_{LLC}	8.33
L_m	151.11 μH
L_r	15.11 μH
C_r	10.48 nF
DC-link voltage range V_b	36–60 V
Non-inverting buck-boost HV HEMTs	EPC2302 (2 in parallel)
Non-inverting buck-boost LV HEMTs	EPC2302 (2 in parallel)
L_{BB}	300 μH

TABLE III: Parameters of the ISOP LLC-DAB.

Parameter	Value
LLC HV HEMTs	IGLD60R070D1
LLC LV HEMTs	EPC2204
n_{LLC}	6
L_m	150.99 μH
L_r	15.10 μH
C_r	10.48 nF
LLC input voltage $V_{in,\text{LLC}}$	288 V
DAB HV HEMTs	IGLD60R070D1
DAB LV HEMTs	EPC2022
n_{DAB}	8.5
L_{DAB}	37.87 μH
DAB input voltage range $V_{in,\text{DAB}}$	24–424 V
DAB nominal input voltage $V_{in,\text{nom,DAB}}$	224 V

III. Power losses

This section details each of the loss factors considered for the comparison. Specifically, the conduction losses P_{cond}, the switching losses P_{sw}, the gate charge losses P_{G}, and the reverse conduction losses P_{SD} are evaluated for all devices [20]. The following equations are derived for a half-bridge having V_A as dc-link voltage and a load current i_B, as shown in Fig. 8.

The conduction losses are due to the internal resistance of the GaN HEMT when a current flows from drain to source. For each device, the internal resistance is obtained from the corresponding datasheet, considering a temperature of $T = 25\,^{\circ}\text{C}$.

$$P_{\text{cond}} = R_{\text{ds,on}} I_{B,\text{RMS}}^2 \tag{20}$$

The switching losses include the turn-on losses P_{on} and the turn-off losses P_{off}. P_{on} are given by the sum of the output capacitance losses P_{oss} and the turn-on overlap losses $P_{\text{on,overlap}}$. P_{oss} is associated to the charging and discharging of the output capacitance C_{oss} of the GaN HEMTs. When the turn-on event is characterized by ZVS, i.e. when the load current charges and discharges C_{oss} within the dead time, P_{oss} is zero. However, for hard-switching events P_{oss} is different from zero and can be calculated as:

$$P_{\text{oss}} = E_{\text{oss,total}} f_s \tag{21}$$

where

$$E_{\text{oss,total}} = V_A Q_{\text{oss,Q2}} \tag{22}$$

In the previous equation, $Q_{\text{oss,Q2}}$ is the total charge on the output capacitance of the device Q2. and it is defined as:

$$Q_{\text{oss,Q2}} = \int_0^{V_A} C_{\text{oss}}(v_{\text{DS}})\, dv_{\text{DS}} \tag{23}$$

The turn-on overlap losses are due to the overlap of the drain-source voltage and the channel current, during the turn-on event, when the voltage decreases to zero and the current increases to reach the load value:

$$P_{\text{on,overlap}} = E_{\text{on,overlap}} f_s \tag{24}$$

where

$$E_{\text{on,overlap}} = \frac{1}{2} V_A I_B (t_{cr} + t_{vf}) \tag{25}$$

and t_{cr} and t_{vf} are the current rise time and voltage fall time, respectively. Reference [20] presents a detailed calculation of t_{cr} and t_{vf}. The turn-off loss P_{off} only includes the overlap losses, during the turn-off event, when the current decreases to zero and the voltage increases to reach the dc-link value:

$$P_{\text{off,overlap}} = E_{\text{off,overlap}} f_s \tag{26}$$

where $E_{\text{off,overlap}}$ is the energy dissipated during one turn-off event. $E_{\text{off,overlap}}$ can be calculated using (27) or (28), depending on whether the gate driver has a high or low gate resistance, respectively, with the latter typically occurring in GaN HEMTs.

$$E_{\text{off,overlap}} = \frac{1}{2} V_A I_B (t_{vr} + t_{cf}) \tag{27}$$

$$E_{\text{off,overlap}} = \frac{1}{12} \frac{(I_B t_{cf})^2}{C_{\text{oss,Q1}}(0) + C_{\text{oss,Q2}}(V_A)} \tag{28}$$

t_{vr} and t_{cf} are the voltage rise time and the current fall time, respectively, and reference [20] details their calculation.

The gate-charge losses P_{G} are due to the accumulation and dissipation of electrical charge Q_{G} on the gate.

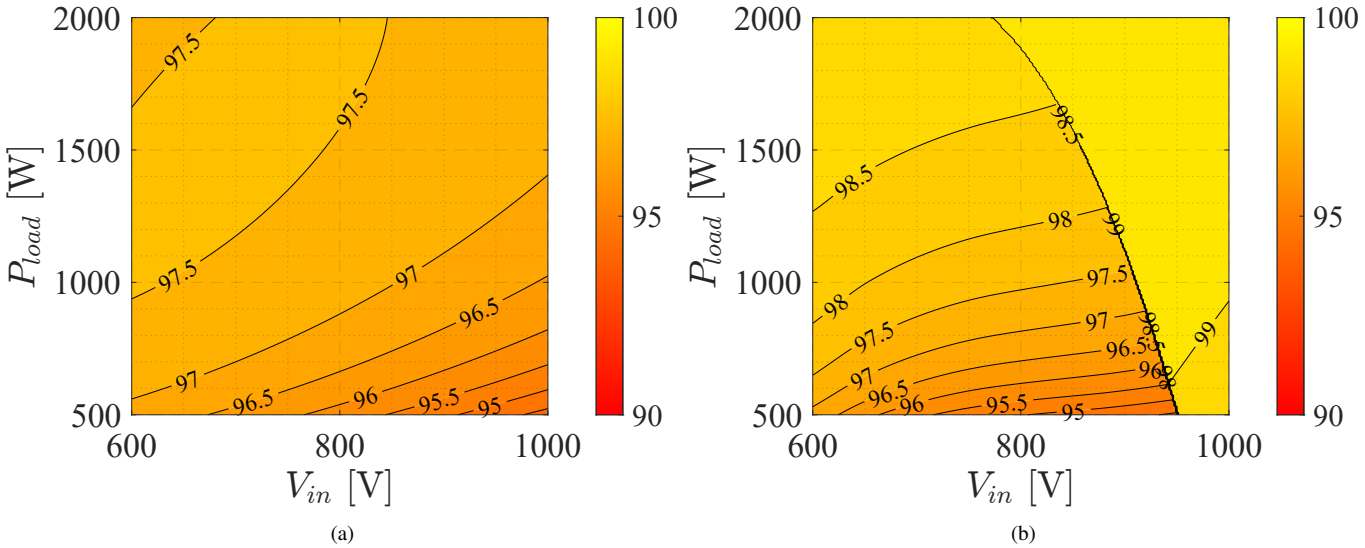
$$P_{\text{G}} = Q_{\text{G}} (V_{\text{g,on}} - V_{\text{g,off}}) f_s \tag{29}$$

where $V_{\text{g,on}}$ and $V_{\text{g,off}}$ are the gate voltage to turn-on and off the HEMT, respectively. Common values for a GaN HEMT are $V_{\text{g,on}} = 5\,\text{V}$ and $V_{\text{g,off}} = 0\,\text{V}$.

Reverse conduction losses P_{SD} exist when a HEMT is off, but the current flows its source to drain terminals, behaving like a freewheeling diode. In this case, a voltage drop V_{SD} exist from source to drain. V_{SD} is specified in the device datasheet as a function of the source-drain current I_{SD}. Once the value of V_{SD} is given, P_{SD} can be calculated according to

$$P_{\text{SD}} = I_{\text{SD}} V_{\text{SD}} t_{\text{SD}} f_s \tag{30}$$

where t_{SD} is the reverse conduction time.



(a) (b)

Fig. 9: Efficiency results for the two topologies: (a) ISOP LLC with non-inverting buck-boost post-regulator, (b) ISOP LLC-DAB.

IV. Comparison Results

The parameters of the ISOP LLC converter with non-inverting buck-boost post-regulator and the ISOP LLC-DAB are reported in Tables II and III, respectively.

In the first topology, the LLC modules work as DCXs. Therefore, the dc link voltage of each LLC varies according to the input voltage V_{in}. The non-inverting buck-boost converter is assumed to operate exclusively in Continuous Conduction Mode (CCM), as the opposite Discontinuous Conduction Mode (DCM) would otherwise alter both the equations of the non-inverting buck-boost and LLC converters, requiring a separate analysis.

In the ISOP LLC-DAB, the output voltage V_{out} is regulated by the DAB. Therefore, the input voltage of the LLC modules $V_{in,\text{LLC}}$ is constant, and calculated through (7), while the input voltage on the DAB module is determined according to

$$V_{in,\text{DAB}} = V_{in} - 2V_{in,\text{LLC}} \tag{31}$$

Fig. 9 presents the efficiency results for both architectures. Overall, the LLC-DAB topology shows a clear advantage in terms of efficiency, particularly when operating near the full power rating. This superior performance can be attributed to the ZVS operating region of the DAB converter, which minimizes switching losses and contributes to the improved efficiency.

Conversely, the LLC with the non-inverting buck-boost post-regulator topology performs better at lower power ratings, achieving 97% efficiency for the lower input voltage values. However, the non-inverting buck-boost converter operates in hard-switching mode throughout the entire load range, resulting in higher switching losses at higher power levels. Consequently, its efficiency decreases significantly at full power, as illustrated in Figs. 10 and 11.

The DAB converter consistently outperforms the buck-boost converter in terms of efficiency, further enhancing the overall performance of the two LLC modules. However, the addition of an extra transformer in the DAB topology increases the weight and volume of the entire converter, which could be a limiting factor in applications where size and weight are critical constraints.

In Fig. 12, the losses are broken down by their sources for both topologies. Specifically, the losses are categorized into conduction, switching, and additional losses, with the latter including the gate driver losses and reverse conduction losses. The graphs should be interpreted vertically: as an example, at the operating point of 500 W and 1000 V, the losses for the two LLC topologies can be broken down into 5% conduction losses, 90% switching losses, and 5% extra losses.

The main difference between the two topologies lies in the distribution of losses between the non-inverting buck-boost and the DAB. Specifically, the DAB operates within a trapezoidal zone where Zero-Voltage Switching (ZVS) is achieved, as indicated by the black line in Fig. 12b. In this region, the switching losses are minimized to 10%. In contrast, the switching losses for the buck-boost converter remain relatively high across the entire operating range, without the significant reduction experienced by the DAB. Moreover, the adoption of the DAB as a regulator improves the conduction and switching losses in the LLC modules.

In conclusion, while the LLC-DAB topology offers a wider operational range with higher efficiency, particularly at higher power levels, the LLC with non-inverting buck-boost post-regulator topology may provide a more compact and efficient solution for low-power applications.

V. Conclusion

This paper presents a comparative analytical analysis of the LLC with non-inverting buck-boost post-regulator and LLC-

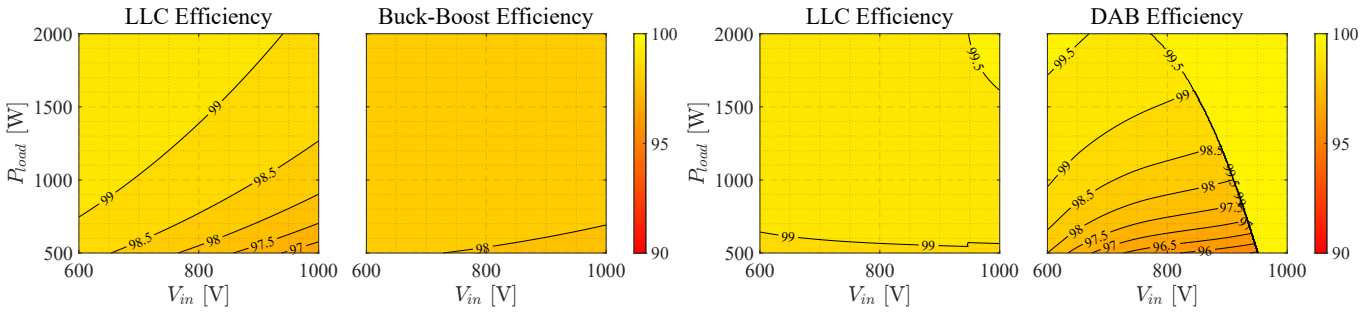


Fig. 10: Partial efficiency of each conversion stage for the two topologies: (a) ISOP LLC with non-inverting buck-boost post-regulator, (b) ISOP LLC-DAB.

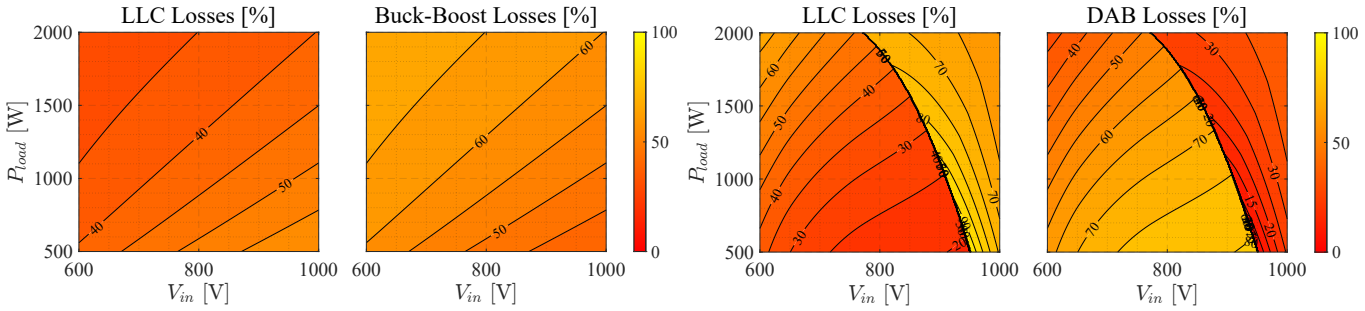


Fig. 11: Losses percentage of each conversion stage for the two topologies: (a) ISOP LLC with non-inverting buck-boost post-regulator, (b) ISOP LLC-DAB.

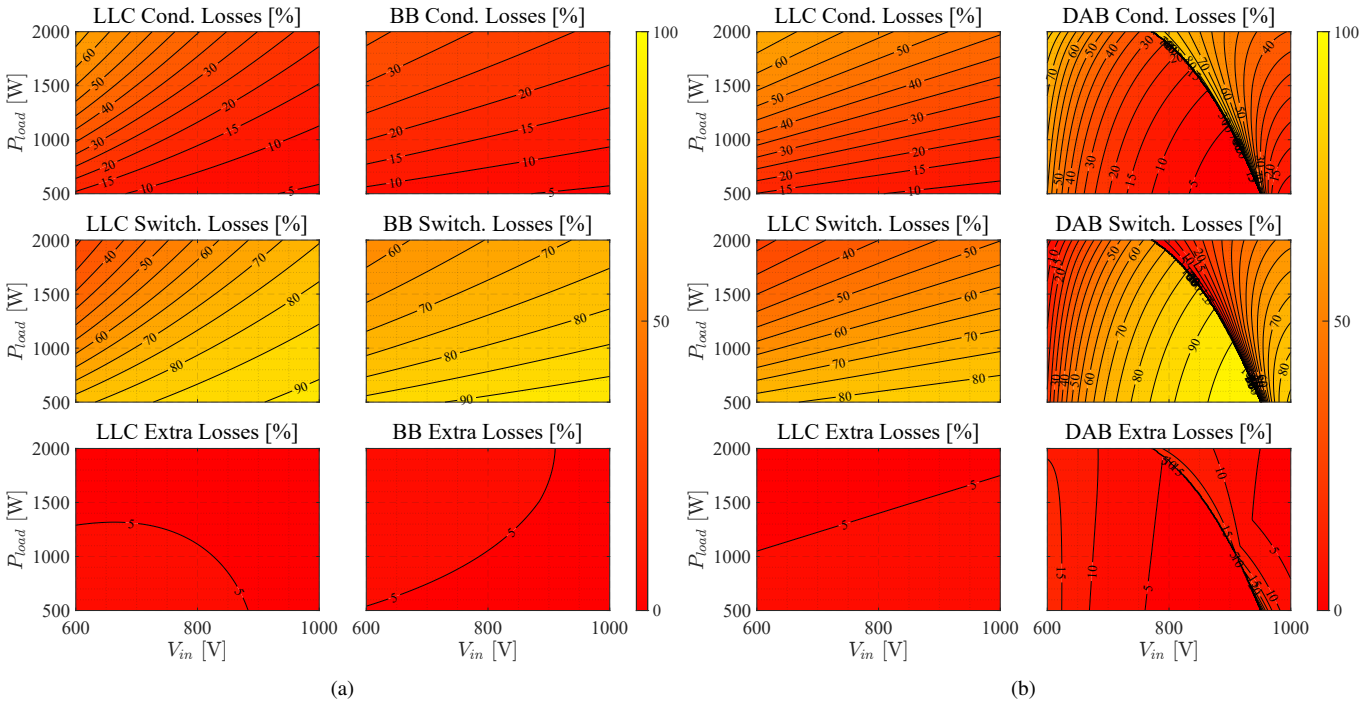


Fig. 12: Percentage of the conduction, switching and additional losses of each conversion stage for the two topologies: (a) ISOP LLC with non-inverting buck-boost post-regulator, (b) ISOP LLC-DAB.

DAB topologies, both in ISOP configurations, with a focus on efficiency and an evaluation of the losses in the GaN devices. The results demonstrated that the LLC-DAB topology achieves higher efficiency, particularly at full power operation, due to the ZVS capability of the DAB converter. This not only reduces switching losses but also enhances the overall performance of the LLC modules.

On the other hand, while the LLC with non-inverting buck-boost post-regulator topology shows competitive efficiency at lower power levels, its hard-switching operation leads to higher losses at full load, making it less efficient under those conditions. Despite its lower efficiency, this topology may offer advantages in terms of size and simplicity.

While this study has focused on efficiency and loss distribution, future research could extend the analysis to power density considerations. Investigating the trade-off between efficiency and size could help determine whether a compromise can be reached between the two topologies, optimizing both performance and power density for specific applications.

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